A REVIEW OF THE USE OF ELECTRO-THERMAL SIMULATIONS FOR THE ANALYSIS OF HETEROSTRUCTURE FETs

Giovanna Sozzi and Roberto Menozzi

Dipartimento di Ingegneria dell’Informazione
University of Parma
Parco Area delle Scienze 181A, 43100 Parma, Italy
Tel. +39-0521-906044, Fax +39-0521-905822, giovanna.sozzi@unipr.it

Abstract

This paper deals with using device-level numerical simulations for the investigation of the electro-thermal behavior of a GaAs-based heterostructure FET. We show a way of dealing with the software/hardware limitations related with the huge disproportion between the electrically active region and the volume relevant to heat outflow. We study very wide simplified structures to obtain guidelines for building up a reduced grid and proper boundary conditions for the complete simulation of the electro-thermal behavior of the FET. As an application example, we use this approach to simulate the military standard (MIL-STD) method for the measurement of the thermal resistance of GaAs FETs, thus discussing its accuracy and limitations. We also show that in multi-finger structures a single channel temperature such as that obtained by electrical thermal resistance extraction techniques cannot satisfactorily describe the FET’s thermal behavior. Finally, we briefly dwell on a comparison between 2D and 3D simulations.

Keywords

Channel temperature, thermal resistance, FETs, Gallium compounds, semiconductor device modeling, heterostructure.
I. INTRODUCTION

The assessment of the thermal behavior of semiconductor devices is a major concern in the semiconductor industry, by no means limited to high-power technologies. In digital circuits, higher and higher levels of integration and clock speeds booster the power dissipated per unit area. On the other hand, analog RF and microwave MMICs show relatively low power efficiencies and in particular GaAs-based circuits suffer from low thermal conductivity (nearly one third of that of Silicon).

The internal temperature of a device (typically referred to as channel temperature for FETs, junction temperature for bipolar devices) impacts on both its performance and reliability. The temperature dependence of physical parameters such as resistivities, carrier concentrations, mobilities, lifetimes, etc., often causes the deterioration of device maximum current, gain, and cut-off frequency with increasing temperature [1]. As far as reliability is concerned, the knowledge of the maximum operating temperature is very important, not only because most failure mechanisms are exponentially accelerated by temperature, but also because the presence of temperature peaks inside the device, the so-called hot spots, can lead to sudden and destructive burn-out.

The thermal characterization of semiconductor devices is therefore crucial for design as well as for reliability estimation purposes.

The literature documents several different methods to analytically evaluate, or to measure the thermal resistance or the channel temperature (we will hereafter refer to the case of a FET).

Analytical methods try to obtain the channel temperature by solving the heat propagation equation, which can only be done for particularly simple structures, heat source geometries, and boundary conditions [2].
On the other hand, thermal resistance measurements are affected by errors that limit their accuracy and repeatability [3], often requiring correction procedures [4]. The accuracy of thermal resistance measurements is very important. Errors of few K in measuring the peak channel temperature can heavily affect the devices lifetime extrapolations [5]. Moreover, the thermal resistance of any specific device varies with temperature (hence with power), and it is influenced by other factors, like the chip layout or mounting methods [6].

All these aspects contribute to the complication of the thermal characterization and management of semiconductor devices.

The purpose of this paper is to review the use of commercial simulation tools for the investigation of the electro-thermal behavior of a semiconductor FET device, and to show how to overcome or deal with the software or hardware limitations related with the huge disproportion between the electrically active region and the volume relevant to heat outflow. As an example, we will focus our analysis on the military standard MIL-STD-750D, method 3104 [7], for the measurement of thermal resistance of GaAs FETs, and we will use the numerical model to estimate its accuracy and limitations.

The structure of this paper is as follows. In section II, we describe the military standard MIL-STD-750D, method 3104. Section III deals with the issue of choosing a simulation grid wide enough to allow reliable thermal resistance evaluation but small enough for the simulations to be computationally efficient (or feasible at all), and we illustrate a method to evaluate the thermal resistance contribution of the semiconductor regions that are left out of the grid. In section IV, the MIL-STD-750D thermal resistance extraction procedure is numerically applied to an AlGaAs/GaAs HFET: the thermal resistance and channel temperature thus obtained are compared with the ones directly given by the
simulations. The following section V touches the issues connected with multi-finger devices, while section VI offers a comparison between 2D and 3D simulations. Finally, section VII concludes the paper.

II. THE MIL-STD-750D METHOD FOR THERMAL RESISTANCE EXTRACTION

We now describe the MIL-STD-750D, method 3104 [7], for thermal resistance testing of GaAs FETs. The experimental set-up is sketched in Fig.1, together with the corresponding waveforms. The circuit consists of a DUT (Device Under Test), a voltage source ($V_H$), a current source ($I_M$), and an electronic switch (S). The forward-biased gate–source junction diode voltage ($V_{GSf}$) is used as a Temperature-Sensitive Electrical Parameter (TSEP).

The method consists of a calibration phase and a measurement phase. During the calibration phase, the S switch is open. A constant forward current, $I_M$, flows through the gate-source diode. In the experiment the DUT has to be placed in a temperature-controlled environment able to keep the device temperature constant within $\pm 1$ K during the calibration procedure, and the case reference temperature has to be measured using a thermocouple with accuracy of $\pm 0.5$ K. The corresponding $V_{GSf}$ is recorded for various ambient temperatures, with resolution of at least 1 mV.

The plot of the measured $V_{GSf}$ values versus temperature is the calibration curve. $I_M$ is chosen so that $V_{GSf}$ is a linearly decreasing function of temperature over the expected temperature range: $I_M$ has to be high enough to forward bias the diode, without introducing significant self-heating. A calibration factor $K_f$ is defined as the absolute value of the reciprocal of the calibration curve slope.
The measurement phase requires $V_{GSf}$ to be measured before ($V_{GSf}(i)$) and after ($V_{GSf}(f)$) the application of a heating pulse, to get the pre- and post-heating junction temperatures. During both measurements the switch is open. During the heating phase the switch is closed, the drain is biased with a voltage $V_H$ while the current $I_M$ is kept constant. The drain heating current $I_H$ is measured. The heating phase lasts for a time $t_H$. Then the switch is opened and $V_{GSf}(f)$ measured. The value of the thermal resistance $R_{TH}$ is then calculated with the following formula:

$$R_{TH} = \frac{\Delta T}{P_H} = \frac{K_P [V_{GSf}(f) - V_{GSf}(i)]}{I_H \times V_H}.$$ 

### III. NUMERICAL SIMULATIONS

We simulated the electro-thermal behavior of an AlGaAs/GaAs HFET by means of a commercial software tool [8]. We focused on the thermal resistance of the die, i.e., that between the channel and the die-attach.

The set-up of Fig. 1 has been reproduced with a mixed-mode simulation, where a 2-D hydrodynamic HFET model including self-consistent solution of the heat flow equation is embedded in a SPICE-like circuit simulation. In order to overcome the convergence problem arising from the presence of the switch, we replaced the $V_H$ voltage source and the switch with a current source $I_D$: during the heating pulse, the current $I_D$ is fixed at a non-zero value, while during the measurement phase it is kept at zero, thus simulating the open-switch (i.e., floating-drain) condition.

The device is an Al$_{0.25}$Ga$_{0.75}$As/GaAs medium-power HFETs fabricated by Alenia-Marconi Systems [9]. It has a 200 µm gate width and a gate length of 0.25 µm. The main DC electrical features are: saturation current $I_{DSS} = 200$ mA/mm (defined at $V_{GS} =$
0, in the saturation region), peak transconductance $g_m \approx 150 \text{ mS/mm}$ (in the saturation region), threshold voltage $V_T \approx -2 \text{ V}$. The off-state drain-gate breakdown voltage is 19-20 V. At 10 GHz and 1-dB compression, the typical power density and gain are 0.6 W/mm and 9.6 dB, respectively.

Unlike electrical simulations, where almost only the active device area (typically spanning just a few microns in either direction) needs to be simulated, the electro-thermal analysis requires the simulation of much bigger structures (tens or hundreds of microns each side), hence the finite-difference simulation mesh ends up having a very large number of nodes, which makes the simulations extremely time consuming and hardware-demanding, and numerical convergence often difficult to reach.

The first question to answer, in order to achieve an accurate and efficient numerical model, is therefore: How can we limit the simulated area to an acceptable value without losing the required accuracy? Or, in other words: What boundary conditions should we use to properly account for the effect of the semiconductor regions lying outside the simulated cross-section?

Thus, we simulated several different structures in order to correlate the thermal resistance with the dimensions of the simulated cross-section and the dissipated power.

The structure in Fig. 2 is a simplified model of the situation where the HFET device on the die surface is acting as a heating contact (“top”) through a heat flow boundary conditions; the back of the die (“bottom”) is at a fixed temperature of 300 K (Dirichlet boundary condition) and acts like a heat sink; adiabatic boundary conditions are applied at the remaining boundaries. Thanks to axial symmetry, only half of the structure needs to be simulated. The top thermal contact length is half the length of the active device area, i.e., 3.5 $\mu$m. The GaAs thermal conductivity is $\kappa = 0.76–0.001 \cdot T$ [W/K/cm], and
the thermal heat capacitance is 1.82+2.5·10^{-4}\text{·}T \text{[J/K/cm}^3\text{]} \text{(neglecting the temperature dependence of } \kappa \text{ results in an error of about 11% on the maximum temperature increase when the peak lattice temperature is in the range of 400 K).}

The peak lattice temperature increment (\Delta T) has been calculated for different combinations of the structure width (A) and depth (B), and for dissipated power densities of 3\cdot10^3 \text{ W/cm}^2 (105 \text{ mW/mm}), 9\cdot10^3 \text{ W/cm}^2 (315 \text{ mW/mm}) and 3\cdot10^4 \text{ W/cm}^2 (1050 \text{ mW/mm}). The \Delta Ts for power densities of 3\cdot10^3 \text{ W/cm}^2 and 3\cdot10^4 \text{ W/cm}^2 are reported in Tab. 1 for the various structures.

Fig. 3 shows the dependence of the simulated peak temperature increase versus the depth (B) of the structure in Fig. 2, for two widths, namely A = 250 \text{ µm} and A = 750 \text{ µm}, and for three values of the power density. As expected, the channel temperature increases as the distance between the top heat source and the bottom heat sink gets longer. However, \Delta T shows the anticipated linear dependence on substrate thickness B only when the latter is equal to or larger than the simulated width A, corresponding to a heat-sink-limited condition.

The dependence of the peak temperature increase versus the width (A) of the structure in Fig. 2 is given in Fig. 4, for two depths, namely B = 250 \text{ µm} B = 500 \text{ µm}, and for the same three values of the power density as seen in Fig. 3. Fig. 4 tells us that, in order for the simulation not to be sidewall-limited, the distance between the heat source and the adiabatic sidewall must be at least equal to the depth of the structure.

Based on these results, in the simulations that follow we set B = 500 \text{ µm}, as a representative value for a non-thinned GaAs wafer, and A = 750 \text{ µm}, in order to avoid a sidewall-limited condition.
Fig. 5 shows the horizontal (solid line) and vertical (dashed line) temperature profile for power densities of $3 \cdot 10^3$ W/cm$^2$, $9 \cdot 10^3$ W/cm$^2$, and $3 \cdot 10^4$ W/cm$^2$. About 30% of the temperature drop, in either direction, falls outside the first 100 µm from the heat source, 20% out of the first 200 µm; therefore, reducing the lateral and/or vertical dimension of the simulated cross-section to values such as these or lower introduces large errors in the estimation of peak temperature, unless the thermal spreading resistance of the regions left out of the simulation is evaluated and properly accounted for in the boundary conditions.

In an electro-thermal device simulation, it is practically impossible to deal with structures as wide as those used so far. Classically, a few microns of material are considered in either direction, with suitable boundary conditions seeking to account for the “outdoors”. In order to reduce the simulation domain, as a first step we calculated the thermal resistance of the structure in Fig. 2 as the ratio between the local increment over the heat-sink temperature and the power density driving the top thermal contact. This helps estimating the errors that result from reducing the complete structure and replacing the substrate regions that cannot be simulated with a suitable lumped thermal resistance.

The thermal resistance between the bottom heat-sink and points along a horizontal and a vertical line (both originating in the top contact) is shown in Fig. 6, for a power density of $3 \cdot 10^4$ W/cm$^2$, as a function of the distance from the heat source.

We assumed that the active device could be considered an almost uniform heat source if compared with the entire die, so we kept only 10 µm of GaAs on the sides of the HFET and under the buffer. The remaining non-simulated GaAs on the device sides and below corresponds to a thermal resistance per unit area of about $1.93 \cdot 10^{-3}$ K·cm$^2$/W, as
obtained from the curve in Fig. 6 (the distance between the surface and the bottom of the simulated area being about 15 µm). A “bottom” thermal contact was therefore introduced to model the thermal flow out of the simulated structure. It defines a non-homogeneous Neumann boundary condition with a surface thermal resistance of 1.93·10^{-3} \text{ K cm}^2/\text{W}. We thus obtained the new simulation structure plotted in Fig. 7 together with an enlargement of the active part of the HFET device.

We biased this reduced structure (Fig. 7) with \( V_{GS} = 0 \) V and with \( V_{DS} \) values yielding the same power densities used in the full structure (Fig. 2, with \( A = 750 \) µm and \( B = 500 \) µm). In Tab. 2 we compare the channel temperature increment (over the ambient temperature of 300 K) obtained in the two structures for the three power densities. The channel temperature of the reduced structure differs from that of the full structure by -0.7 K (out of 9.1 K) for 3·10^3 \text{ W/cm}^2, 0.9 K (out of 27.6 K) for 9·10^3 \text{ W/cm}^2, and 6.7 K (out of 100.3 K) for 3·10^4 \text{ W/cm}^2. This makes us confident enough about the ability of the reduced structure to simulate the essential features of heat dissipation of the full structure.

We believe that the reason why in Table 2 the temperature increase in the reduced structure is smaller than that of the full structure at low power/temperature and larger at high power/temperature is that by replacing the semiconductor surrounding the reduced structure with a single thermal resistance in series with the bottom contact, we are to some extent changing the geometry of the heat flow. In particular, the semiconductor lying at the sides of the reduced structure can be thought to act as a thermal resistance in parallel. The contribution of this lateral “shunt” thermal resistance can be expected to be larger at high power/temperature, because the thermal resistance of the central part (the reduced structure) is somewhat larger due to higher lattice temperature. Therefore, we
can expect the temperature increase to be somewhat overestimated at high power/temperature, as shown in Table 2.

IV. SIMULATION OF THE MIL-STD METHOD

In order to simulate the application of the MIL-STD method for thermal resistance extraction [7], we connected the HFET structure of Fig. 7 in a mixed-mode configuration to current sources at the drain and gate electrodes, as described in section III.

First we started with the calibration step, as described in section II. With the drain disconnected ($I_D = 0$), the gate was driven with a positive $I_{GS} = I_M = 10^{-2}$ mA/mm, and the simulation was repeated for different ambient temperatures. The corresponding $V_{GS}$ values were reported vs. the ambient temperature to obtain the calibration curve shown in Fig. 8. The calculated calibration factor is $K_f = 822$ K/V.

We then simulated the thermal measurement step. Prior to the power pulse, i.e. with drain disconnected, the same measurement current $I_M$ of the calibration step ($10^{-2}$ mA/mm) has been applied to the gate, and the gate-source voltage drop $V_{GS}(i)$ has been recorded to have a measurement of the initial junction temperature. Then a 3-s heating pulse has been applied with a drain-source heating current $I_D = 325$ mA/mm, and the corresponding $V_{DS}$ value has been recorded. The $I_D$ pulse rise and fall times were 200 ns. After the pulse, we recorded the $V_{GS}(f)$ value.

Fig. 9 shows the maximum lattice temperature ($T_{LMAX}$, dashed line) as well as $V_{GS}$ (solid line) plotted versus time for a heating current $I_D = 325$ mA/mm. Time = 0 marks the beginning of the heating current pulse fall. From 0 to 200 ns, the fall of $I_D$ makes
$V_{GS}$ decrease accordingly until, when the $I_D$ pulse is over, $V_{GS}$ starts increasing gently as the device cools down. The peak value of $T_{LMAX}$ ($T_{LMAX,HEAT}$) was 314.0 K.

The instant at which the $V_{GS}(f)$ value has to be taken is very critical. We define the measurement delay time $t_{MD}$ as the time elapsed from the beginning of the trailing edge of the heating current pulse to the moment when we record $V_{GS}(f)$. $t_{MD}$ has to be out of the electrical transient following the switching-off of the current source, but short enough to correctly detect the maximum temperature reached inside the device during the heating pulse. Being the $I_D$ pulse fall time $t_{fall} = 200$ ns, we started recording $V_{GS}(f)$ with increasing $t_{MD} > t_{fall}$.

Starting from the end of the switch-off transient of $I_D$ ($t_{MD} = 200$ ns), we have recorded $V_{GS}(f)$ at different times and extracted the maximum lattice temperature ($T_{LMAX,VGS}$) from the increment over room temperature ($T_{room} = 300$ K) calculated using the MIL-STD method, with the following expression:

$$(T_{LMAX,VGS} - T_{room}) = K_f \cdot |V_{GS}(f) - V_{GS}(i)|.$$  

The extracted temperature ($T_{LMAX,VGS}$) for a heating current $I_D = 325 mA/mm$ is shown in Fig. 10 (open squares) as a function of the measurement delay time $t_{MD}$. In the same figure we also report the maximum lattice temperature ($T_{LMAX,SIM}$) as obtained directly from the simulation. The temperature found with the simulated MIL-STD method tracks the maximum lattice temperature at the time of the $V_{GS}(f)$ measurement within 0.5 K, indicating that the calibration is accurate.
We then compared the maximum lattice temperature ($T_{L\text{MAX-}V\text{GS}}$) obtained with the simulated MIL-STD method with the maximum temperature $T_{L\text{MAX-HEAT}}$ reached inside device at the end of the heating pulse.

The errors reported in Fig. 11 vs. the measurement delay time $t_{\text{MD}}$ are defined as

$$\varepsilon = (T_{L\text{MAX-HEAT}} - T_{L\text{MAX-}V\text{GS}}).$$

As one can observe, the minimum $\varepsilon$ (Fig. 11) is 5.5 K, and the error increases with the measurement delay time reaching 9.1 K after 2 $\mu$s and 10.5 K after 5 $\mu$s.

V. MULTI-FINGER DEVICES

Another problem arises when characterizing multi-finger devices: it is well-known that the temperature is far from being uniformly distributed among the fingers, the inner ones being significantly hotter than the outer ones due to less efficient heat removal. A single channel temperature or thermal resistance value such as that yielded by the MIL-STD technique or, for that matter, any other electrical technique, cannot therefore accurately describe the thermal conditions inside the device.

As an example, Fig. 12 shows the simulated temperature profile along the right half of a 12-finger HFET structure (thanks to device symmetry, simulation of the left half is redundant). The heating areas corresponding to the gate fingers are 7 $\mu$m wide and 7 $\mu$m apart, and the power density is $10^4$ W/cm$^2$. The channel temperature increase is 246 K under the hottest (central) fingers, but only 189 K under the coldest (outermost) ones. Under conditions such as these it is obviously hard to attach a physical meaning to a single channel temperature, and accurate analytical models or numerical simulations are the only alternative to microscopy techniques.
If we define a single thermal resistance based on the channel temperature of the hottest finger, the area-normalized thermal resistance is necessarily an increasing function of the number of fingers, as Fig. 13 shows for 5 values of power density (from $0.5 \cdot 10^4$ W/cm$^2$ to $1.5 \cdot 10^4$ W/cm$^2$ with a step of $0.25 \cdot 10^4$ W/cm$^2$). This finding is consistent with experimental results (see for instance [10]). Simulations and charts such as these are necessary to properly scale the devices and their models.

VI. 3D SIMULATIONS

Although two-dimensional (2D) simulations are by far the most common tool used for physical modeling of electro-thermal phenomena in semiconductor devices, the phenomena themselves are of course three-dimensional (3D); therefore, it is necessary to estimate the error made by neglecting 3D effects, i.e., by considering a device with infinite width in the z-direction (the dimension orthogonal to the simulated cross-section). For a fixed power density, we can expect the maximum temperature of the 3D structure to be lower than that of the 2D simulation due to heat dissipation in the z-direction, and to tend to the maximum temperature of the 2D simulation as the device width increases and tends to infinity. This means that the 2D results always represent a worst-case situation, and therefore have a value of their own even when no 3D analysis tool is available.

It is an obvious remark that the computational overhead problems of 2D electro-thermal simulations are wildly exacerbated in 3D; for instance, it would be impossible to simulate an HFET structure such as ours in 3D with the mesh refinement required to model the layer structure and the heterointerfaces with acceptable accuracy, while at the same time retaining the minimum volume of surrounding semiconductor necessary for
thermal outflow modeling. We have thus limited our 3D analysis to solving for the
temperature distribution in a simplified structure where, as described in section III, the
HFET is replaced by a uniform power source. The 3D simulation volume is shown in
Fig. 14. Assuming a 200-µm-wide HFET, such as those studied here [9], the symmetry
of the structure allows limiting the analysis to one half (the 100 µm top contact of Fig.
14), if we replace the plane of symmetry with an adiabatic sidewall. For the other
sidewall, shaded in gray in Fig. 14, we have applied either constant-temperature (300 K)
or adiabatic boundary conditions, as described below.
To begin with, we wanted to make sure that the 3D structure gave results identical to the
2D structure under identical thermal conditions, i.e., that the differences observed
between 3D and 2D were not numerical artifacts due to different meshing. So, we
simulated the volume in Fig. 14 with a 200 µm heat source contact along the whole
depth and adiabatic sidewalls: this situation is clearly equivalent to simulating a 2D
cross-section such as those described in section III. For a power density of \(3 \times 10^4\) W/cm\(^2\),
we found a peak lattice temperature of 399.9 K in 3D, versus a value of 400.3 K in 2D.
This made us confident enough that the 3D mesh did not introduce numerical
inconsistencies.
We then simulated the temperature distribution in the 3D structure corresponding to a
power density of \(3 \times 10^4\) W/cm\(^2\), for the two cases of adiabatic and constant-temperature
(300 K) sidewall (the gray surface of Fig. 14). The surface temperature profiles are
shown in Fig. 15. With an adiabatic sidewall, the peak temperature, corresponding to
the center of the 200 µm device, is 381.7 K (distance = 0 in Fig. 15), while the edge of
the contact (distance = 100 µm in Fig. 15) is at 346.8 K. These temperatures decrease to
371.8 K and 336.5 K, respectively, with a constant-temperature sidewall at 300 K. As recalled above, the corresponding temperature in the 2D structure is about 400 K. Our simulations therefore indicate that the 2D analysis overestimates the peak channel temperature in a 200 µm FET by something in the range of 20-30 K for a temperature increase of 70-80 K over room T, corresponding to a power density of $3 \cdot 10^4$ W/cm$^2$ (180 mW integrated over the whole 7x200 µm$^2$ active device area). Also, under these conditions, the difference between the maximum and the minimum temperature along the 200 µm FET is in the range of 35 K.

VII. CONCLUSION

This paper gives an account of the usefulness as well as the difficulties of using device-level numerical simulation tools for the investigation of the electro-thermal behavior of a semiconductor FET device (namely, a GaAs-based heterostructure FET). We showed a way of overcoming or dealing with the software or hardware limitations related with the huge disproportion between the electrically active region and the volume relevant to heat outflow. We studied very wide (e.g., 500x750 µm$^2$) simplified structures to obtain guidelines for building up a reduced grid and proper boundary conditions for the complete physical simulation of the electro-thermal behavior of the FET.

We applied this approach to the simulation of the military standard MIL-STD-750D, method 3104, for the measurement of thermal resistance of GaAs FETs, and used the numerical model to estimate its accuracy and limitations.
A study of the temperature distributions in multi-finger structures showed that a single channel temperature such as that obtained by electrical thermal resistance extraction techniques cannot describe the thermal behavior of the FET with satisfactory accuracy. Finally, a comparison between 2D and 3D simulations has shown that the former can significantly overestimate the maximum channel temperature and obviously neglect temperature differences along the device depth (the dimension that is not simulated in the 2D structures) that can be a large part of the peak temperature rise.

Numerical approaches such as that shown in this paper, together or in place of analytical methods or microscopic investigation techniques, are therefore a necessary tool for the analysis and prediction of the device electro-thermal behavior and its impact on performance and reliability.
REFERENCES


TABLE CAPTIONS

Tab.1: Peak lattice temperature increment for the structure of Fig. 2. Different combinations of width (A) and depth (B) have been simulated for two power densities at the top contact, namely $3 \cdot 10^3$ W/cm$^2$ and $3 \cdot 10^4$ W/cm$^2$. N/C indicates that no numerical convergence could be reached.

Tab.2: Peak lattice temperature increment reached in the reduced structure of Fig.7 and in the full structure (Fig. 2, A = 750 µm, B = 500 µm) for different power densities.
Tab.1

<table>
<thead>
<tr>
<th>B</th>
<th>50 µm</th>
<th>250 µm</th>
<th>500 µm</th>
<th>750 µm</th>
<th>Power Density [W/cm²]</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 µm</td>
<td>5.9</td>
<td>5.6</td>
<td>5.6</td>
<td>5.6</td>
<td>3·10³</td>
</tr>
<tr>
<td>250 µm</td>
<td>15.2</td>
<td>8.2</td>
<td>8.0</td>
<td>7.9</td>
<td></td>
</tr>
<tr>
<td>500 µm</td>
<td>27.2</td>
<td>10.5</td>
<td>9.2</td>
<td>9.1</td>
<td></td>
</tr>
<tr>
<td>750 µm</td>
<td>39.516</td>
<td>12.901</td>
<td>10.418</td>
<td>9.831</td>
<td></td>
</tr>
</tbody>
</table>

| 50 µm | 63.2  | 60.0   | 59.4   | 59.3   | 3·10⁴                 |
| 250 µm | 188.2 | 90.3   | 87.1   | 87.0   |                       |
| 500 µm | N/C   | 120.0  | 103.0  | 100.3  |                       |
| 750 µm | N/C   | 152.5  | 118.2  | 110.5  |                       |
Tab. 2

<table>
<thead>
<tr>
<th>Power Density [W/cm²]</th>
<th>Reduced Structure (Fig. 7)</th>
<th>Full Structure (Fig. 2)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ΔT [K]</td>
<td>ΔT [K]</td>
</tr>
<tr>
<td>3·10³</td>
<td>8.4</td>
<td>9.1</td>
</tr>
<tr>
<td>9·10³</td>
<td>28.5</td>
<td>27.6</td>
</tr>
<tr>
<td>3·10⁴</td>
<td>107.0</td>
<td>100.3</td>
</tr>
</tbody>
</table>
FIGURE CAPTIONS

Fig. 1: Measurement set-up and waveforms for the MIL-STD thermal resistance extraction technique [7].

Fig. 2: Simplified structure with a surface heat source (“top” contact) and a bottom heat-sink (“bottom” contact). We have simulated various combinations of width (A) and depth (B).

Fig. 3: Peak temperature increase in the structure of Fig. 2 vs. the depth B, for three values of the power density at the top heat source contact, for $A = 250 \, \mu m$ (closed symbols) and $A = 750 \, \mu m$ (open symbols).

Fig. 4: Peak temperature increase in the structure of Fig. 2 vs. the width A, for three values of the power density at the top heat source contact, for and $B = 250 \, \mu m$ (open symbols) and $B = 500 \, \mu m$ (closed symbols).

Fig. 5: Horizontal (closed symbols) and vertical (open symbols) temperature profile for three values of the dissipated power density. Both the horizontal and the vertical lines along which temperatures are recorded originate in the top contact.

Fig. 6: The thermal resistance between the bottom heat-sink and points along a horizontal (closed symbols) and a vertical line (open symbols) (both originating in the top contact) for a power density of $3 \cdot 10^4$ W/cm².
Fig. 7: Simulated HFET structure and enlargement of the active area of the simulated structure.

Fig. 8: Simulated calibration curve for a gate-source current $I_M = 10^{-2}$ mA/mm and drain floating.

Fig. 9: Simulated time dependence of the maximum lattice temperature (dashed line) and $V_{GS}$ (solid line) for a heating current $I_D = 325$ mA/mm. Time “zero” is the time when the heating current pulse starts falling down.

Fig. 10: Maximum lattice temperature vs. measurement delay time $t_{MD}$: $T_{LMAX, SIM}$ (closed symbols) is the maximum lattice temperature as given by the simulation, while $T_{LMAX, VGS}$ (open symbols) is the channel temperature yielded by the simulated MIL-STD extraction technique.

Fig. 11: Temperature error vs. measurement delay time $t_{MD}$. This chart refers to the same simulation as Fig. 9 and Fig. 10.

Fig. 12: Simulated maximum lattice temperature increment along a horizontal axis in a 12-finger FET. Owing to device symmetry, we simulated only the right half of the device. The surface heat sources corresponding to the gate fingers are 7 µm wide and 7 µm apart. The power density is $10^4$ W/cm$^2$. 
Fig. 13: Simulated specific thermal resistance as a function of the number of gate fingers, for different values of the power density. The surface heat sources corresponding to the gate fingers are 7 \( \mu \text{m} \) wide and 7 \( \mu \text{m} \) apart. The power density is (bottom to top) \( 0.5 \cdot 10^4 \text{ W/cm}^2 \) to \( 1.5 \cdot 10^4 \text{ W/cm}^2 \) with steps of \( 0.25 \cdot 10^4 \text{ W/cm}^2 \).

Fig. 14: 3D simulated structure. The “top” thermal contact is the heating source; the bottom surface is kept at 300 K; the gray sidewall is either adiabatic or kept at 300 K; the top surface and remaining sidewalls are adiabatic.

Fig. 15: Lattice temperature along the AA’ line of the 3D structure of Fig. 14. The sidewall thermal contact of Fig. 14 is either adiabatic or kept at a constant temperature of 300 K. The power density is \( 3 \cdot 10^4 \text{ W/cm}^2 \).
Fig. 1
Fig. 2

"top" thermal contact

GaAs

"bottom" thermal contact

A

B
Fig. 3

\[ \Delta T [K] \]

- \( P = 3 \times 10^4 \text{ W/cm}^2 \)
- \( P = 3 \times 10^3 \text{ W/cm}^2 \)
- \( P = 9 \times 10^3 \text{ W/cm}^2 \)

Heat source distance from bottom [m]

\( \text{? m} \)
Fig. 4

heat source distance from lateral sidewall [m]

$\Delta T [K]$

$P = 9 \cdot 10^3 W/cm^2$

$P = 3 \cdot 10^4 W/cm^2$

$P = 3 \cdot 10^3 W/cm^2$
Fig. 5

- Horizontal cut
- Vertical cut

\[ T_{\text{LMAX}} \text{ [K]} \]

- Pd = \( 3 \cdot 10^4 \text{W/cm}^2 \)
- Pd = \( 9 \cdot 10^3 \text{W/cm}^2 \)
- Pd = \( 3 \cdot 10^3 \text{W/cm}^2 \)

Distance [?m]
Fig. 6

$R_{TH} [\text{mK cm}^2/\text{W}]$

- horizontal cut
- vertical cut

Distance [m]
Fig. 7
slope = 1/Kf
Kf=822 K/V
Fig. 10
Fig. 11
Fig. 12

\[ \Delta T \text{ [K]} \]

\[ \text{horizontal distance [m]} \]

T\text{room}=300 \text{ K}
Troom=300 K

$R_{TH}$ [mK·cm$^2$/W]

Power density

number of fingers

Fig. 13
Fig. 14
Fig. 15