Experimental and numerical study of the recovery softness and overvoltage dependence on p-i-n diode design

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**Short title:** softness and reverse recovery overvoltage in P-i-N diodes

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Abstract

This work offers a reliability-oriented characterization of power p-i-n diodes turn-off transients. The softness of the turn-off and the snap-off voltage (defined as the threshold beyond which large, anomalous reverse overvoltages develop across the diode at turn-off) are investigated both experimentally and numerically for a wide set of diodes with different drift region width, resistivity and lifetime. In particular, lifetime control is obtained by electron irradiation at different doses. As a result, guidelines emerge for the design of the snubberless diode with optimum trade-off between switching speed and softness. It is also suggested that, for complete diode characterization, the well-known softness factor be accompanied by the snap-off voltage, i.e. the peak reverse voltage triggering anomalous oscillations in the turn-off transient.

Keywords: Power diodes, reverse recovery, electron irradiation
1 Introduction

Fast recovery diodes play a key role in topical power electronics circuits as freewheeling, snubber or clamp diodes. However, the excellent switching performance of new power semiconductor switches, like IGBT’s, impose very hard turn-off condition to the diodes, with fast current gradients that may result in large overvoltages. Optimal diode design for these applications should therefore offer a satisfactory trade-off among features such as: (i) a soft recovery, which limits overvoltages and oscillations; (ii) low reverse recovery current ($I_{RR}$), to allow a high $dI/dt$ diode capability at turn-off; (iii) low energy losses during recovery. The first requirement is particularly important, since p-i-n fast-recovery power diodes must typically be used in conjunction with snubbers that limit the dangerous overvoltages caused by steep current ramps, which can damage the diode itself and the surrounding elements. Due to the complexity and cost of snubber circuits and the lack of uniformity of the solutions adopted by the manufacturers, p-i-n power diodes able to withstand snubberless operation are extremely desirable. In this respect, the problem is that of designing diode structures ensuring self-limitation of the peak reverse voltage at the moment of current switch-off [1-5].

With reference to a simple inductive switching arrangement, Fig. 1 depicts the snubberless reverse recovery transient of a p-i-n diode. In the reverse recovery phase, a large reverse current flows through the diode. In the first part of the transient ($t_A$) the decrease of the current is forced by the external circuit, with a constant ($dI_D/dt)_1$, down to the maximum reverse current value $I_{RR}$; meanwhile, the diode voltage is practically that of the forward-bias steady-state. During in the second part of the recovery transient ($t_B$), the current rapidly approaches zero, with a slope ($dI_D/dt)_2$, which depends on ($dI_D/dt)_1$ and on the device structure. In the meantime, the voltage starts decreasing and reaches the peak reverse voltage $V_{PK}$, corresponding to the
maximum value of the positive current gradient, \((dI_D/dt)_{2\text{max}}\), before getting to the reverse steady-state value \(V_R\). Obviously,

\[ V_{PK} = V_R + L_R (dI_D/dt)_{2\text{max}}. \]  \hspace{1cm} (1)

The shape of the reverse recovery current transient shows remarkable variations from diode to diode: *hard* diodes feature a steep current rise at the end of the transient and, consequently, a large negative overvoltage; *soft* diodes, on the other hand show a slower current rise and a lower overvoltage. As will be shown in the following (see for instance Fig. 4), the steep \((dI_D/dt)_2\) of hard switching conditions results in a much larger negative overvoltage and undesirable, wide oscillations at the end of the transient, which may represent a reliability issue [2,6,7].

In order to quantify the diode behavior during recovery, a parameter called *softness* or S-factor is usually defined as follows (see for instance [8]):

\[ S = t_B / t_A. \]  \hspace{1cm} (2)

A small S-factor means a hard diode and, typically, large reverse overvoltages at turn-off.

In this standard approach, however, the value of \(t_B\) is typically extracted assuming a linear current rise during \(t_B\), which is a drastic simplification; moreover, the S-factor is not directly linked with the negative overvoltage, which is the main reliability issue connected with the diode’s turn-off.

A different approach was therefore introduced in a previous work [9], starting from the experimental evidence that, in a snubberless circuit, and for values of \((dI_D/dt)_1\) that do not produce anomalous oscillations, there is a linear dependence between the peak reverse voltage and \((dI_D/dt)_1\), which can be written as:

\[ V_{PK} - V_R = L_R |(dI_D/dt)_1| / S. \]  \hspace{1cm} (3)

Comparing eq. (1) and eq. (3), the definition of the softness is then modified as follows:
\[ S = \left| \frac{(dI_D/dt)_1}{(dI_D/dt)_{2\text{max}}} \right|, \]

and then, from eq. (3) and from the measurement of \( V_{PK} \) and \( (dI_D/dt)_1 \), in a circuit with a known \( L_R \), the S-factor can be evaluated as:

\[ S = L_R \left| \frac{(dI_D/dt)_1}{(V_{PK} - V_R)} \right|. \]  

In this framework, the purpose of this work is the study of the reverse recovery softness as a function of the diode’s design, including in particular an investigation of the anomalous overvoltage oscillations arising for large \( \left| (dI_D/dt)_1 \right| \). Both experimental and numerical simulation techniques have been used. The final target is a set of design indications for diodes featuring an optimal speed/softness trade-off.

2 Experimental results

2.1 Samples

The devices under test are press-packed p-i-n single diodes, manufactured starting from n-type \(<1,1,1>\) Neutron Transmutation-Doped (NTD) 100 mm Silicon wafers. High-temperature Gallium and Phosphorus diffusion was used to achieve the proper p-i-n structure. The thickness of the \( p^+ \) and \( n^+ \) layers is 80 \( \mu m \) and 60 \( \mu m \), respectively. For lifetime control we used electron irradiation in a 12 MeV linear accelerator and a range of standard doses [10]. The monotonic decrease of \( \tau \) with increasing dose was verified by means of Open Circuit Voltage Decay (OCVD) measurements [11]: for example, in the diodes with \( W_i = 235 \mu m \) (samples C, E and G) we measured, in the absence of electron irradiation, lifetimes ranging from 100 to 250 \( \mu s \) (at 25 °C), which dropped to about 2 \( \mu s \) for the maximum irradiation dose (50 kGy). The wafers were laser-cut to a diameter of 31 mm and then alloyed on a Molybdenum substrate, Gold-
plated and encapsulated into press-pack ceramic housings. The effective diameter of the active area is about 24 mm.

With the purpose of extracting the effect of physical and structural parameters such as intrinsic base resistivity ($\rho$), width ($W_i$) and carrier lifetime ($\tau$) on the reverse recovery behavior, devices with different intrinsic base length, doping and irradiation dose were designed and fabricated, as reported in Tab. 1. The features in Tab. 1 were chosen to span the typical ranges used in fast power diode manufacturing.

2.2 Measurements

For the turn-off transient characterization, the device under test (DUT) was inserted in the circuit of Fig. 2. The left part of the circuit generates, when $T_1$ is turned on, a sinusoidal current wave that forward-biases the DUT; after a quarter of a period, when the peak current value (which depends on the initial condition on $C_1$) is reached, $T_2$ is turned on and the diode’s turn-off transient starts. One can set the negative current slope ($dI_D/dt)_1$ at the desired value by varying $L_2$ and/or the initial condition on $C_2$ ($V_{2(0)}$).

We measured the reverse recovery transient for all the samples in Tab. 1, using values of the inductance $L_2$ ranging from 1 to 4 $\mu$H and different $V_{2(0)}$’s. Fig. 3 shows the values of the peak reverse voltage $V_{PK}$ measured during the reverse recovery with $L_2 = 1 \mu$H, for different values of ($dI_D/dt)_1$ (obtained varying $V_{2(0)}$). The dependence of $V_{PK}$ on ($dI_D/dt)_1$ can be split into two regions (separated by a transition region): one where a linear relationship holds, followed by one where the peak voltage soars. We will refer to the latter condition as snap-off.

The waveforms measured at points I, II, and III, located in the linear, transition, and snap-off regions, respectively, are shown in Fig. 4. The condition labelled as I corresponds to a soft-recovery transient, with relatively low overvoltage and strong damping of the voltage
oscillations following the negative voltage peak. In case II, the turn-off behavior tends to become hard (the overvoltage increases) and the damping of the spurious oscillations is slower. Finally, under condition III an anomalous, very large negative overvoltage arises, and the oscillations are wider and last longer; such a behavior can easily damage the diode itself or the surrounding circuitry and must be regarded as a serious reliability hazard.

These three situations (I to III) have been observed in most of the samples listed in Tab. 1 (in some instances, the $V_{PK}$ values of case III exceeded the instrumentation range and could not be measured). We found that the snap-off voltage $V_S$ (defined as the threshold value of the negative peak voltage, beyond which we enter the type III behavior) depends on the diode’s technological features, but not on the value of the inductance $L_2$. $V_S$ is therefore a peculiar feature of the DUT, and a very important one for its safe operation: it should therefore be quoted in the data sheets together with the softness factor $S$.

2.3 S-factor dependence on temperature and technological parameters

The S-factor was measured for all of the samples at two different junction temperatures: 25 °C and 125 °C, the latter being considered the typical device temperature under normal operating conditions. Experimental (as well as simulated) data show an increase of the softness with temperature, due to higher carrier lifetimes. A more detailed temperature analysis carried out on two diodes (from lots C and I) in the 25-150 °C range, showed a roughly linear increase of $S$ with $T$, with a slope of $3-4 \times 10^{-4} \, ^\circ C^{-1}$. This implied, for the diodes under test, an increase of $S$ of about 15 % from 25 °C to 150 °C.

The influence of the irradiation dose on the softness varies with resistivity and base width, as shown in Fig. 5 for $T = 125 \, ^\circ C$. At relatively high resistivity and thickness (E and G samples), the S-factor decreases with irradiation dose, due to shorter carrier lifetimes. When
base resistivity and thickness are smaller (lots A and B), the lifetime value becomes less critical, and the effect of the irradiation dose is hardly significant.

As far as the dependences of S on the base width and resistivity are concerned, Fig. 6 summarizes the results obtained (at 125 °C) on diodes with the same irradiation dose (15 kGy). The measured dependence on \(W_i\) is non-monotonic. It is worth noting that a very similar \(W_i\) dependence has been observed for the lifetimes (as extracted by OCVD measurements) of the samples of Fig. 6, which vary by about 20 % over the whole range of base width values. This moderate dispersion of the \(\tau\)’s and, consequently, the one observed in Fig. 6 for the S-factor, should therefore be attributed to small differences in the starting material of the different lots. To the best of our present knowledge, no conclusion can be drawn about the influence of \(W_i\) on S, except that, once the difference among the lifetimes has been accounted for, this influence should be minor in the range of base widths that we explored. Finally, for a fixed value of \(W_i\), the S-factor is a weakly growing function of \(\rho\) (Fig. 6). This finding can again be connected with the lifetime values: lower doping (i.e., higher resistivity) implies longer lifetimes, hence larger S-factors. However, also the dependence of S on \(\rho\) can be considered quite weak.

3 Numerical simulations

Since in regions II and III (as defined in Fig. 3 and Fig. 4), where the diode peak reverse voltage dramatically increases, the voltage compliance of the experimental set-up allows to measure only a few samples, for a thorough study of the snap-off behavior we relied on numerical simulations, performed using a commercial tool. In the next paragraphs, we will briefly describe the software tool we employed, and present and discuss the main simulation results.
3.1 Simulation tool

Since the turn-off diode’s behavior depends on a combination of diode’s and switching circuit’s features, we used a mixed-mode simulation technique, whereby the active device is simulated using a finite-element method and a drift-diffusion model, while the surrounding circuit is treated in a SPICE-like fashion.

We simulated various diode structures among those listed in Tab. 1. The doping profile and geometrical dimensions were the same as those of the real device. The effect of the different electron irradiation doses was rendered changing the high-injection carrier lifetime (\(\tau\)); for each simulated structure we used the \(\tau\) value that we measured on the corresponding diode using the OCVD technique. For the irradiation doses of Tab. 1, the experimental values of \(\tau\) range from 1.4 \(\mu\)s to 251 \(\mu\)s.

For the sake of numerical convergence, the circuit we used in the simulations (shown in Fig. 1a) is simpler than that used in the measurements (Fig. 2), but at the same time it retains the essential features of inductive switching.

3.2 Numerical investigation of the snap-off behavior

In this section, we show and discuss the results of simulated turn-off transients with different values of \((dI_D/dt)_1\). We performed these simulations on the whole set of diodes listed in Tab. 1 both at 25 and 125 °C. As an example, we show here the results of sample B6 (featuring \(W_i = 110 \, \mu\)m, \(\rho = 120 \, \Omega \, \text{cm}, D = 5 \, \text{kGy}\) at 25 °C; in this diode the different types of turn-off behavior (I to III) are quite evident, but they can be clearly observed in most of the simulated structures.

Type I behavior
In Fig. 7a we show the simulated reverse-recovery transient obtained for sample B6 with \((dI_D/dt)_1 = - 65 \text{ A/\mu s}\). This kind of behavior is what we referred to as type I. The frequency of the damped oscillations is practically constant and equal to the resonance frequency of an LC circuit \((1/(2\pi (L C)^{1/2}))\), where \(L = L_R\) and \(C\) is the capacitance due to the depleted region of the reverse-biased diode. Indeed, from our simulations we get, for the reverse-biased diode capacitance during the turn-off transient, an average value \(C = 1.16 \text{ nF}\) \((C = A \varepsilon_s / W_d, \text{ where } A \text{ is the area, } \varepsilon_s \text{ the dielectric constant for Si, and } W_d \text{ is the depletion width extracted by the simulations})\). Together with the inductance value \(L_R = 0.967 \text{ \mu H}\), this \(C\) would give a resonance frequency of 4.75 MHz, in close agreement with the one observed in Fig. 7a (4.5 MHz). This simple resonant behavior can be observed also in SPICE simulations, using a standard p-n diode model: the oscillation frequency is that determined by the product of the circuit inductance and the depletion capacitance of the diode’s model.

**Type II behavior**

If we increase \(|(dI_D/dt)_1|\) up to 69 A/\(\mu\)s, the behavior of the reverse recovery of sample B6 turns into one of type II, as shown in Fig. 7b. In this case, the positive half-waves of the voltage oscillations are clipped by the diode’s turn-on, and the current behavior gets saw-tooth-like. As in case I, this sort of behavior can be observed also in SPICE simulations using the p-n diode standard model.

**Type III behavior**

If we further increase the negative current slope of the current, a value is reached \((- 71 \text{ A/\mu s for diode B6})\) where an anomalous overvoltage appears, as illustrated by Fig. 7c. This is what we called the snap-off region, or type III behavior, a kind of turn-off transient that, unlike the other two, cannot be simulated by SPICE using the standard p-n diode model, and is specifically linked with the p-i-n structure of the DUT. By looking at the carrier distributions at
different time points during the transient simulation (Fig. 8), we found that the snap-off is triggered when the diode reverse voltage is large enough for the drift region to be completely depleted. A parallel look at Fig. 7c and Fig. 8 shows that, from a smooth voltage rise at point (1), where the drift region is not yet totally depleted, the diode snaps to a sharp, very large overvoltage at (2), when the depletion region reaches the n⁺ cathode layer. This observation has been confirmed by DC reverse-bias simulations, which give a punch-through voltage (V_{PT}) very close to the snap-off voltage V_S (440 V and 430 V, respectively), as already observed in other works [12,13].

Other simulated diodes showed a somewhat different snap-off behavior, in that the snap-off starts after the negative voltage peak, as illustrated in Fig. 9 for sample B2 (W_i = 110 µm, ρ = 120 Ωcm, D = 0 kGy) at 125 °C and for (dI_D/dt)_1 = -137 A/µs. We investigated the carrier and electric field distributions in the device during this transient: Fig. 10 shows the situation at two different time points (marked by (1) and (2) in Fig. 9). It clearly appears that the maximum of the electric field corresponds to the peak voltage (point (1)) but, due to the rapidity of the transient, at this time the depleted zone has not reached the limit of the drift region yet. The drift region gets completely depleted at point (2), where the anomalous overvoltage occurs. This observation further confirms the link between the onset of snap-off and the complete depletion of the drift region.

### 3.3 Influence of the technological parameters on the snap-off behavior

Since the importance of the snap-off voltage characterization has been established, an understanding of its dependence on the diode’s technological features is mandatory for optimum device design.
Starting from the structure of one of the measured samples (A8), with $W_i = 110 \, \mu m$, $\rho = 63 \, \Omega cm$, $D = 1.5 \, kGy$, and varying, from case to case, one of these three technological parameters, we simulated (at a junction temperature $T = 25 \, ^{\circ}C$) the reverse-recovery transient at increasing values of $|dI_D/dt|$, until the snap-off condition was reached.

Fig. 11a shows the results of the simulations performed with different values of the drift region resistivity. A clear decrease of $V_S$ appears as $\rho$ is increased. Such dependence is due to the increase of $V_{PT}$ with the doping concentration of the drift region: as the doping is reduced (and the resistivity gets larger) a smaller reverse bias is required to deplete the whole drift region. Since we have seen that $V_S$ and $V_{PT}$ are tightly correlated, the behavior of Fig. 11a is not surprising.

Given this link between $V_S$ and $V_{PT}$, we also expect the former to increase with $W_i$, because the complete depletion of the drift region is reached for larger reverse bias. This is confirmed by the simulations, as shown in Fig. 11b.

A less straightforward and more interesting result was found by varying $\tau$ (to simulate the different irradiation doses). Higher lifetimes give rise to larger snap-off voltages, as plotted in Fig. 11c. Once more, the tight connection between $V_S$ and $V_{PT}$ sheds some light on the results. For longer lifetimes, the mobile charge stored in the drift region is less affected by recombination during the turn-off transient, and a larger reverse voltage is required for total depletion; on the other hand, short lifetimes imply that a substantial amount of stored charge is lost in recombination during the transient, hence a lower reverse bias is necessary to deplete the whole $n^-$ region.

Wherever available (as mentioned above, $V_S$ sometimes exceeds the set-up measurement range), the experimental results confirmed the trends of Fig. 11. As an example, experimental
Vs values for samples with $W_i = 110 \, \mu m$, $\rho = 63 \, \Omega cm$, increased from about 400 V to 770 V for measured $\tau$ values ranging from 5 $\mu s$ to 65 $\mu s$.

4 Conclusions

We can now draw a few indications as to the choices one should make in order to design an optimum device from the snap-off point of view. It emerges from Fig. 11 that a high-Vs diode should have a wide, high-doping and non-irradiated (i.e., with $\tau$ as large as possible) drift region. Long lifetimes also tend to result in diodes with a soft turn-off behavior, but clearly collide the requisite of fast operation (demanding a short $\tau$). Moreover, the reduction of the power loss in forward mode would require small values of $W_i$. The optimum design will therefore come from a suitable trade-off between the performance required by the particular application and overvoltage/reliability considerations. The drift-diffusion/SPICE simulations represent a powerful tool in the search for this trade-off.

In conclusion, for a characterization of the turn-off transient that does not overlook important reliability considerations, the power p-i-n diodes used in snubberless applications need to be accompanied by two figures, namely, the softness factor S, which directly relates to the negative overvoltages taking place during inductive switching, and the snap-off voltage, that marks the onset of dangerous oscillations in the reverse recovery waveforms and the occurrence of very large, potentially destructive overvoltages across the diodes.

By considering both experimental results and drift-diffusion/SPICE numerical simulations performed on a wide range of p-i-n diode structures, we have investigated the softness and snap-off behavior and we have correlated it with technological features such as resistivity, width and electron irradiation dose (i.e., carrier lifetime) of the drift region.
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References


**FIGURE CAPTIONS**

*Fig. 1 -* a) A simple circuit used to study a diode’s inductive switch-off behavior; $R = 1$ mΩ, $L_R = 0.967$ μH, $I_F = 100$ A. b) Diode current and voltage transients during switch-off.

*Fig. 2 -* Test circuit used for the experimental characterization of the reverse recovery.

*Fig. 3 -* Measured peak reverse recovery voltage versus $|dI_D/dt|_1$ (as defined in Fig. 1) for one of the devices under test. Points I, II, and III mark three different situations located in the linear, transition, and snap-off regions, respectively.

*Fig. 4 -* Measured reverse recovery voltage (solid lines) and current (dashed lines) transients at points I, II, and III (as defined in Fig. 3).

*Fig. 5 -* Measured dependence of the softness factor $S$ on the electron irradiation dose, for different diode lots (defined in Tab.1).

*Fig. 6 -* Measured dependence of the softness factor $S$ on the intrinsic base width $W_i$, for different diode lots (defined in Tab.1).

*Fig. 7 -* Simulated current (solid lines) and voltage (dotted lines) reverse recovery of sample B6 ($D = 5$ kGy) at $T = 25$ °C: (a) type I behavior, obtained for $(dI_D/dt)_1 = -65$ A/μs; (b) type II behavior, obtained for $(dI_D/dt)_1 = -69$ A/μs; (c) type III behavior, obtained for $(dI_D/dt)_1 = -71$ A/μs.
Fig. 8 - Simulated electron (dashed line) and hole (dotted line) distributions, and electric field (solid line) inside the diode, at time points (1) and (2) of Fig. 7c. The drift region extends from 80 µm to 190 µm.

Fig. 9 - Simulated current (solid lines) and voltage (dotted lines) reverse recovery of type III in sample B2 (D = 0) at T = 125 ºC, \((dI_D/dt)_1 = -137 \text{ A/µs.}\)

Fig. 10 - Simulated electron (dashed line) and hole (dotted line) distributions, and electric field (solid line) inside the diode, at time points (1) and (2) of Fig. 9. The drift region extends from 80 µm to 190 µm.

Fig. 11 - Dependence of the simulated snap-off voltage \(V_S\) on the intrinsic base (a) resistivity \(\rho\), (b) width \(W_i\), and (c) carrier lifetime \(\tau\). The simulations are carried out at \(T = 25 ^o\text{C.}\)
## Tables

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<tr>
<th>Sample Lot</th>
<th>Intrinsic base Resistivity $\rho$ [Ω cm]</th>
<th>Intrinsic base Width $W_i$ [µm]</th>
<th>Irradiation Dose $D$ [kGy]</th>
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Table 1. Technological features of diodes under test.
(a) 

(b) 

P. Cova et al. – Fig. 1
P. Cova et al. – Fig. 6
P. Cova et al. – Fig. 7a
P. Cova et al. – Fig. 10
Figure 11

(a) $V_s$ [V] vs $\rho$ [Ωcm]

(b) $V_s$ [V] vs $W_i$ [μm]

(c) $V_s$ [V] vs $\tau$ [μs]