Hot Electron Effects on Al$_{0.25}$Ga$_{0.75}$As/GaAs Power HFET’s Under Off-State and On-State Electrical Stress Conditions

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Abstract—This work shows a detailed comparison of the degradation modes caused by off-state and on-state room temperature electrical stress on the dc characteristics of power AlGaAs/GaAs heterostructure field effect transistors (HFET’s) for X- and Ku-band applications. The devices are stressed under dc bias conditions that result in electron heating and impact ionization in the gate-drain region. Incremental stress experiments carried out at gate-drain reverse currents up to 3.3 mA/mm (for a total of more than 700 h) show a remarkably larger degradation for the off-state stress, due to more pronounced electron heating at any fixed value of gate reverse current. This represents an important piece of information for the reliability engineer when it comes to designing the accelerated stress experiments for hot electron robustness evaluation. The degradation modes observed, all of a permanent nature, include threshold voltage and drain resistance increase and drain current and transconductance reduction.

I. INTRODUCTION

Today, an urgent demand exists for amplifiers able to deliver, at X- and Ku-band (10–15 GHz) or above, output power in the range of several watts or tens of watts for wireless communication system portable units and land and space base stations, respectively. This makes the development of power field effect transistors (FET’s) with large gate-drain breakdown voltage (BV) of paramount industrial importance in the race for this huge-volume market. Large values of BV are indeed necessary because 1) increasing the FET output power by using large-periphery devices leads to FET input and output impedances too low to get a good match with the surrounding circuits; and 2) since power-added efficiency is critical for portable units, the amplifying FET’s must be operated under class AB or B conditions, i.e., with large quiescent drain-gate voltage ($V_{DG}$).

Unfortunately, a tradeoff exists between BV and the FET conductance, because a negative surface potential over the gate-drain access region, which is beneficial for the breakdown, degrades the open-channel saturation current ($I_{DSS}$), transconductance ($g_m$) and rf power gain. Consequently, the design and characterization of high-BV GaAs-FET’s are very hot topics nowadays [1]–[3].

In this framework, heterostructure FET’s (HFET’s), where an n-AlGaAs layer is grown on top of a relatively high-doping n-GaAs channel, potentially offer a good compromise for the industrial production of high-power FET’s [4]–[7]. In comparison with GaAs MESFET’s, HFET’s offer a larger input voltage swing due to higher Schottky barrier and a better tradeoff between $I_{DSS}$ and breakdown voltage, due to low doping of the AlGaAs barrier layer [8]. Over GaAs pseudomorphic HEMT’s, they feature, in addition to much easier epitaxial growth, improved linearity, due to low AlGaAs doping and the absence of parasitic conduction therein, and larger current capability, since the channel thickness is not limited by the critical value for pseudomorphic growth.

A consequence of the need to bias power FET’s at high $V_{DG}$ is that the most stringent reliability issues are typically due to the large electric fields in the drain-gate region. These are responsible for both off-state and on-state breakdown; the former (also known as closed-channel or two-terminal breakdown) is the drain-gate diode breakdown occurring with pinched-off channel, while the latter (open-channel or three-terminal breakdown) is typically due to high electron conditions and impact ionization in the channel when the device is on. Significant drifts of the electrical characteristics may occur when the devices are biased under such high electric field conditions [9]–[11]. Whether the actual reliability bottleneck is connected with off-state or on-state breakdown depends on the device material and structure [12], as well as on the operating conditions.

When it comes to qualifying devices and setting safety limits for their operation, however, the off-state breakdown voltage ($BV_{OFF}^{D_DG}$) is traditionally more popular than the on-state breakdown voltage ($BV_{ON}^{D_DG}$). $BV_{OFF}^{D_DG}$ is easier to define and measure (it basically involves consideration of the gate-drain diode reverse characteristics, although three-terminal techniques exist [13]), but more careful estimates of the high-field reliability risks need to take into account the actual load line that the instantaneous operating point sweeps during device operation, and determination of $BV_{ON}^{D_DG}$ is also mandatory [14].

The present work aims at a systematic comparison of the effects of off-state and on-state room temperature electrical stress of AlGaAs/GaAs power HFET’s. Such a comparison has a clear practical relevance, in that it provides the reliability engineer with indications as to the quantitative and/or qualitative differences between the degradation modes and mechanisms brought
about by the two stressing modes. Moreover, different experimental techniques are used here in order to gain insight of the physical mechanism underlying breakdown and degradation.

II. SAMPLES AND EXPERIMENTS

A. HFET Structure and Technology

The devices studied in this work (see Fig. 1 for a schematic cross-section) were fabricated using a double-recess process for power HFET’s in production at Alenia Systems Laboratories, with the following bottom-up structure: GaAs SI substrate; AlGaAs/GaAs multilayer buffer; 75 nm thick n-GaAs channel, Si-doped at $10^{17}$ cm$^{-3}$; Al$_{0.25}$Ga$_{0.75}$As barrier layer, Si-doped at $10^{17}$ cm$^{-3}$, 30 nm thick under the gate; n$^+$-GaAs cap for low-resistance ohmic contacts.

The gate metallization has a 0.2 $\mu$m Ti layer with a 0.45 mm Al cap on top. After recess formation by wet etching, 1 $\mu$m long Ti/Al gates are deposited, then the gate length is reduced by selective lateral dry-etching of the Ti, to form a T-shaped gate with the desired footprint length ($L_g$). HFET’s with $L_g$ ranging from 1 to 0.25 $\mu$m are routinely fabricated with this nonlithographic submicron process. The gate width is $W_g = 200$ mm (4 x 50 $\mu$m). The measured gate barrier height is $\Phi_B = 0.81$ eV. The source contacts are connected via air bridges. The deep gate recess is 1 $\mu$m wide and the source-drain spacing is 5 $\mu$m. The passivation is a 300 nm plasma-deposited SiN layer.

Throughout this work, we will refer to HFET’s with $L_g = 0.7$ $\mu$m, featuring typical values of saturation current $I_{DSS} = 300$ mA/mm, transconductance $g_m = 150$ mS/mm and threshold voltage $V_T$ between $-2.5$ and $-3$ V. At 10 GHz and 1-dB compression point, they deliver about 0.5 W/mm output power, with a power gain in the range of 8.5 dB. The off-state drain-gate breakdown voltage ($BV_{D^C}$), defined at 1 mA/mm gate reverse current, with source floating, ranges from 14.2–16.4 V. A safety-limit three-terminal condition is conventionally defined biasing the device close to pinch-off ($I_D = 1$ mA/mm) at a $V_{DS}$ value such that the gate reverse current is 0.1 mA/mm; the corresponding $V_{DS}$ values range from 10.9–12.6 V, with $V_{GS}$ between $-3.5$ and $-4$ V. The data measured in this fashion correspond to drain-gate voltages in the 14.3–16.7 V range (i.e., they give safety figures very close to the $BV_{D^C}$ values quoted above).

B. Experimental Techniques

The dc electrical characterization and stress cycles were carried out using HP-4155 and HP-4142 semiconductor parameter analyzers. 1-ms pulse measurements were also performed with the HP-4142 in order to strip off thermal effects from the DC data.

For the $g_m$ frequency dispersion measurements, we used a setup based on a Schlumberger 1255 HF Frequency Response Analyzer. A small-signal voltage wave of frequency $f$ is superimposed on the dc bias applied to the gate of the transistor under test (biased in the linear region) and the small-signal voltage on the drain resistance is measured. The ratio between the amplitudes of the output and input voltage waves gives a number proportional to $g_m(f)$. Temperature-dependent $g_m(f)$ measurements and current-mode deep level transient spectroscopy (I-DLTS) allowed us to extract the activation energy of deep-levels present in the virgin device or created by the stress.

We also performed an electroluminescence (EL) characterization of the HFET’s, using a single photon counting setup with high-resolution spectral analysis in the energy range 1–3 eV [15].

C. Off-State and On-State Breakdown

Fig. 2 shows the output characteristics of one of our HFET’s. The negative output conductance observed at high $V_{GS}$ is a well-known consequence of self-heating, as demonstrated by the 1-ms pulse measurements (dashed lines), whereby the negative slope is significantly reduced.

The gate reverse current ($I_G$) is universally used as an indicator of both off-state and on-state breakdown. In the former case, the two-terminal drain-gate reverse $I_G$ may originate from impact ionization or tunnelling and thermionic-field emission [16], while in the latter the $I_G$ component due to holes generated by impact ionization in the channel is always dominant [17]. In our case, measurements between $T = -50$ and 70°C give for $BV_{D^C}$ (defined at $I_G = -1$ mA/mm) a roughly linear
dependence on $T$, with a positive coefficient (about 0.012 V/$^\circ$C) which is evidence that the off-state breakdown $I_{G}$ originates from impact ionization. This temperature dependence is also typical of on-state breakdown that is clearly due to impact ionization in the channel.

The reverse $I_{G}$ can typically be correlated with device degradation. Thus, we have superimposed on the output curves of Fig. 2 the constant-$I_{G}$ contours taken at $-0.1$, $-0.5$, and $-1$ mA/mm. Also shown is a possible load line. Getting as much output power as possible, which implies to sweep high-$V_{DS}$ regions of the plane, conflicts with the need to avoid large-$I_{G}$ conditions likely to lead to degradation or failure. In this respect, the areas lying on the right of the $-0.1$, $-0.5$, and $-1$ mA/mm contours, respectively, represent increasingly critical regions. The high-$V_{DS}$ region of the output plane is magnified in Fig. 3. For $I_{D} < 5$ mA/mm, the device is practically pinched off and $I_{G}$ is that of off-state breakdown. For instance, if we take the usual threshold $I_{G} = -1$ mA/mm, Fig. 3 indicates at pinch-off a drain-source BV of 12.45 V (correspondingly, $V_{GS} = -2.79$ V, hence $V_{DG} = 15.24$ V). As $I_{D}$ is increased and the channel opens, the electron concentration in the channel grows, impact ionization starts contributing to $I_{G}$ and the constant-$I_{G}$ contours bend backward toward lower $V_{DS}$ values, i.e., a lower $V_{DS}$ is required to get the same $I_{G}$. If we keep opening the channel up, however, we get to a point where the reduction of the peak electric field (roughly proportional to $V_{DG} = V_{DS} - V_{GS}$) takes over; consequently, the impact ionization rate decreases and the constant-$I_{G}$ contours bend forward, because larger $V_{DS}$ is now required to get the same $I_{G}$.

The shape of the constant-$I_{G}$ contours has important implications on the choice of a safe load line for rf operation. With reference to Fig. 3, let us assume that a safety limit of $-0.5$ mA/mm has been set for rf operation. If only off-state breakdown is considered, as often happens during device qualification, the load line shown in the figures does not seem to pose reliability problems, since it intersects the horizontal axis at $V_{DS} = 10$ V, while the $V_{DS}$ giving $I_{G} = -0.5$ mA/mm under off-state conditions (i.e., zero $I_{D}$) exceeds 12 V. However, as $V_{GS}$ and $I_{D}$ grow and the instantaneous bias point climbs the load line, the device trespasses the $-0.5$ mA/mm $I_{G}$ contour, thus operating, during part of the rf period, outside the safe area. The above considerations therefore indicate that drawing plots like those of Figs. 2 and 3 is mandatory for an accurate evaluation of the device safe operating region and breakdown conditions.

An equivalent way of looking at this matter is shown in Fig. 4. At $V_{GS} < -3$ V, the device is pinched off and $I_{G}$ rapidly grows with $V_{DG}$ (off-state breakdown). For $V_{GS} \approx -2$ V, instead (on-state breakdown), we observe the typical impact ionization-dominated bell-shaped $I_{G}$ curves [17].

### D. Stress Procedures

In order to inspect the robustness of our devices under hot electron conditions and to compare off-state and on-state high-field degradation, we have applied two methods of step-stress tests, hereafter indicated as hot electron stress (HES) and high reverse current (HRC), respectively.

In HES, $V_{GS}$ is fixed at the peak of the $I_{G}$–$V_{GS}$ bell-shaped curve of the virgin device (Fig. 4), while $V_{DS}$ is increased by 0.25 V at each step, starting from 5.5 V. The HRC stress, instead, is carried out with source floating (since three-terminal and two-terminal conditions tend to coincide as the channel is pinched off) and driving the gate-drain diode with a reverse current equal to the $I_{G}$ measured, at the corresponding step, during HES.

All tests were carried out at room temperature. Each step had a duration of 25 h.

Fig. 5 shows the $I_{G}$ value corresponding to each step of both HES and HRC, together with the dissipated power ($P_{D}$). In the upper horizontal axis we reported the $V_{DS}$ applied in HES and the $V_{DG}$ measured in HRC. It is worth noting that 1) the gate reverse current increases more than linearly from step to step, consistently with its impact ionization origin; and 2) $V_{DG}$ is much higher, at each step, in HRC than in HES (since the peak of the $I_{G}$–$V_{GS}$ bell-shaped curves of Fig. 4 is around $-2.2$ V, the $V_{DG}$ value of each HES step can be approximately calculated reading the corresponding $V_{DS}$ value on the top horizontal axis
of Fig. 5 and adding 2.2 V to it), thereby causing larger electric fields and more pronounced carrier heating in the former. It is also important to highlight that we investigated the reliability of our devices in a range of gate currents (up to 3.3 mA/mm) which extends well beyond the widely-accepted reverse safety limit of 1 mA/mm, hence biasing the HFET’s under extreme conditions. It should finally be pointed out that a forward gate current stress with in excess of 4 mA/mm did not produce any device degradation. This proves that the degradation phenomena observed after HRC and HES are not due to the sheer gate current density but to the hot electron and impact ionization conditions.

The stress experiments were stopped after 725 h; the corresponding final $V_{DD}$ values are 14.7 V for HES and 21.9 V for HRC. At the end of HES, $P_D = 180$ mW. At this power level, neglecting the temperature-induced degradation becomes questionable.

### III. EXPERIMENTAL RESULTS AND DISCUSSION

Several electrical parameters have been measured at the end of each HES and HRC step. Tables I and II summarize their changes at two intermediate steps ($I_G = -0.1$ and $-1$ mA/mm) and at the end ($I_G = -3.3$ mA/mm) of HES and HRC, respectively. The main degradation modes are described and discussed in this section. All of them are of a permanent nature: no recovery whatsoever was observed, neither at room temperature nor after 24 h of storage at 150°C.

#### A. Drain Resistance

As shown by Fig. 6 and Tables I and II, by the time the stress $I_G$ reaches $-1$ mA/mm, we measure an increase of the drain parasitic resistance, $R_D$, (as measured using an “end resistance” technique [18]) of 0.4 Ω for HES and 0.65 Ω for HRC (6.8 and 11.4%, respectively). The $R_D$ change increases up to 8.5% (HES) and 53% (HRC) after the total 725 h, when $I_G = -3.3$ mA/mm.

This increase of $R_D$ can be attributed to an accumulation of negative charge in the gate-drain access region, possibly associated with an increase of the surface state concentration caused by impact ionization [9], [19], [20]. The negative charge extends the surface depletion over the gate-drain access region, causing a more resistive path for the electrons that travel toward the drain.

As can be expected, since electron heating mostly takes place at the drain end of the gate (where the electric field peaks), the source-gate access region is almost unaffected by hot electron and impact ionization conditions, and we observe no significant change of the source parasitic resistance $R_S$, as documented by Tables I and II and by Fig. 6.
The creation of new surface states during the stress is confirmed by the increase of the frequency dispersion of $g_m$. Fig. 7 shows the $g_m$ frequency dependence (quiescent bias point: $V_{DS} = 300$ mV, $V_{GS} = 0$ V) measured after several HRC steps (a similar behavior has been observed during HES). The increased surface state concentration widens the area whose depletion is modulated by the gate signal and the $g_m(f)$ dispersion is thus enhanced [21], [22]. Temperature-dependent $g_m(f)$ measurements at the end of HRC, illustrated by Fig. 8, allowed us to extract for the surface states an activation energy $E_a = 0.31$ eV and a cross-section $\sigma = 3.88 \times 10^{-17}$ cm$^{-2}$.

In support of these results, we also carried out, under the same conditions (i.e., for the same device at the end of HRC), an I-DLTS measurement, the results of which are shown in Fig. 9. The analysis of the DLTS peak, which is absent in the virgin devices, gives (see inset of Fig. 9) $E_a = 0.36$ eV and $\sigma = 2 \times 10^{-17}$ cm$^{-2}$ for the trap activation energy and cross-section, respectively, in good agreement with the $g_m(f)$ results.

B. Drain-Gate Off-State Breakdown Voltage

The creation of surface states by impact ionization leads to a beneficial effect on $BV_{DS}^{OFF}$ (measured leaving the source floating and forcing $I_G = -1$ mA/mm through the gate-drain diode). As reported in Fig. 10 (and in Tables I and II for the relative changes), $BV_{DS}^{OFF}$ has increased by 5 V (from 13.5 to 18.5 V) and by 7.5 V (from 14.60 to 22.1 V) at the end of HES and HRC, respectively. This effect is the so-called “breakdown walkout” [9], [23], [24]. No significant change has been observed on the gate-source breakdown voltage $BV_{GS}$ (Tables I and II and Fig. 10), which confirms that surface states are created and electrons are trapped only over the gate-drain access region, where the electrons are hottest.

C. Threshold Voltage

The threshold voltage ($V_T$) is not affected by either HES or HRC for $|I_G| < 2.2$ mA/mm (550 h). For larger gate current magnitudes, we observe a significant increase of $V_T$ (i.e., $V_T$ becomes less negative). At the end of the stress, the relative change
of \( V_T \) is 5\% for HES and 23.9\% for HRC. Trap creation and/or electron trapping in the AlGaAs barrier layer (where DX centers exist [25]) or at heterointerfaces has been shown to produce positive \( V_T \) shifts after hot electron stressing of GaAs PHEMT’s [22].

**D. Drain Saturation Current**

We observed a reduction of \( I_{DSS} \) as well (measured at \( V_{DS} = 2 \text{ V}, V_{GS} = 0 \text{ V} \)), which is a consequence of the increased \( R_D \) and \( V_T \) values. The relative change of \( I_{DSS} \) is 2\% for HES and 7.2\% for HRC up to \( |I_G| = 1 \text{ mA/mm} \) and 6.6 and 31.6\%, respectively, at the end of the stress (\( I_G = -3.3 \text{ mA/mm} \)).

**E. Transconductance**

Our data also show a reduction of the peak \( g_m \) (measured in the linear region, at \( V_{DS} = 100 \text{ mV} \)) by 4.9 and 19.6\% for HES and HRC, respectively, up to \( |I_G| = 1 \text{ mA/mm} \), while the degradation increases to 14.8 and 34.8\%, respectively, at the end of the stress. Smaller degradation is observed for the transconductance measured in the saturation region (see Tables I and II). This is another known effect of the reduction of the surface potential between gate and drain and of the attendant increased depletion; since it degrades the rf power gain as well, it is commonly known as *power slump* [26]–[29]. The larger degradation measured at low \( V_{DS} \) is consistent with this interpretation, since the impact of \( R_D \) is larger in the linear region.

**F. Comparison Between HES and HRC**

From the stress results described above we can conclude that HES and HRC basically induce the same degradation phenomena on our HFET’s (as stated above, the degradation is permanent in both cases). The HRC degradation rate is higher, though, because of larger electric fields attained between gate and drain. Furthermore, during each HES step \( I_G \) slightly decreases, because of the \( I_D \) reduction and \( V_T \) increase, the former lowering the concentration of electrons available for impact ionization, the latter shifting the \( V_{GS} \) where impact ionization peaks from the \( V_{GS} \) stress value; moreover, as breakdown walks out during the stress step, the impact-ionization-dominated gate current tends to decrease. On the other hand, in the HRC case, \( I_G \) is fixed during the stress, so no self-alleviation of the device degradation takes place.

Evidence of the different energy of carriers involved in the two stress experiments has been sought by an EL analysis. Keeping a constant reverse \( I_G = -0.25 \text{ mA/mm} \), the same virgin device was biased in a diode configuration, i.e., with source floating, and at the top of the ionization bell (Fig. 4) with source grounded. These two configurations correspond to the HRC and HES stress conditions, respectively. The two EL spectra are plotted in Fig. 12. The two-terminal bias condition gives a lower total emission intensity, due to a smaller number of carriers involved (the channel is pinched-off), but the larger electric field leads to a higher carrier temperature (5800 versus 3600\text{ K}). This confirms that the degradation effects observed during HRC are stronger because of higher carrier energy. It is also worth pointing out that the presence of an EL peak at about 1.4 eV in the HES curve is a typical signature of impact ionization in the channel, since it is due to band-to-band recombination, in the source region, of cold electrons and holes generated by impact ionization [15], [30]. The secondary peak placed slightly above 1.6 eV has been recently associated with hole capture by DX centers in the Al\(_{0.25}\)Ga\(_{0.75}\)As layer [25].

**IV. Conclusions**

In this work, we have shown a detailed comparison of the degradation modes caused by off-state and on-state room
temperature electrical stress on the dc characteristics of power AlGaAs/GaAs HFET’s for J-band applications. Both off-state and on-state breakdown have been shown to pose potential reliability concerns depending on the device quiescent bias point, class of operation and load line. It is therefore mandatory to assess the device degradation under both conditions.

The devices have been stressed under dc bias conditions that result in electron heating and impact ionization in the gate-drain region, either in a two-terminal configuration with source floating (off-state stress) or in an open channel situation (on-state stress). At each stress step, the gate reverse current was the same for the two stress configurations. Incremental stress experiments carried out at gate-drain reverse currents up to 3.3 mA/mm (for a total of more than 700 h) have shown a remarkably larger degradation for the off-state stress, due to more pronounced electron heating at any fixed value of gate reverse current, as verified by electroluminescence measurements. This represents an important piece of information for the reliability engineer when it comes to designing the accelerated stress experiments for hot electron robustness evaluation.

The degradation modes observed are all of a permanent nature, consistently with experimental evidence that they are mainly due to creation of trap centers. They include threshold voltage and drain resistance increase and drain current and transconductance reduction. The trap levels responsible for the main degradation effects have been characterized measuring the frequency dependence of the transconductance as well as by means of current-mode DLTS experiments.

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REFERENCES

devices such as MESFET’s, HEMT’s, HFET’s, and HBT’s. The reliability evaluation of compound semiconductor and heterostructure electron and characterization, and the dc, rf, and noise characterization, modeling, and study of latch-up in CMOS circuits, IC testing, power diode physics, modeling and hot electron effects in Si and III–V based devices. He has authored or co-authored several book chapters, more than one hundred technical papers in international journals, and more than 100 conference papers in the above mentioned fields.

Dr. Canali has been a member of the Technical Program Committees of several international conferences and is a member of AEI.