Layout Dependence of CMOS Latchup

ROBERTO MENOZZI, LUCA SELMI, ENRICO SANGIORGI, MEMBER, IEEE, GIUSEPPE CRISENZA, TIZIANA CAVIONI, AND BRUNO RICCÒ, MEMBER, IEEE

Abstract—This paper presents a detailed analysis of CMOS latchup dependencies on layout and geometrical dimensions. To this purpose test structures have been fabricated featuring buttied contacts and guard rings with different values of critical distances. The devices have been experimentally characterized in the triggering and sustaining regime, and numerical simulations have been extensively used to interpret the experimental data. It is shown that great care should be taken in designing protection structures since larger areas do not always lead to enhanced latchup immunity.

I. INTRODUCTION

MANY different solutions have been proposed to reduce the latchup susceptibility of CMOS integrated circuits [1]. Among these, epitaxial layers on a heavily doped substrates [2], buttied contacts at the source of the transistors [3], and the use of guard rings [4] are commonly regarded as the most effective and easy to apply. However, while epi-layers have been widely characterized, a detailed quantitative analysis of guard rings and buttied contacts has not yet been presented in the literature.

This paper investigates how layout details influence the latchup characteristics of a standard n-well bulk CMOS technology. Different possibilities have been considered to this purpose, including swapped positions of emitter-base diffusions, buttied contacts, and guard rings. For each of these cases some representative distances (base width of the lateral bipolar transistor, the overall p+ to n+ spacing, etc.) have been varied to investigate their effect on latchup characteristics. The experimental results show that protection structures with larger area occupation do not always lead to reduced latchup susceptibility, as a consequence of different current distributions within the semiconductor.

The experimental results have been qualitatively interpreted by means of the simple lumped element equivalent circuit of Fig. 1, whose parameters (shunting resistances $R_{p}$ and $R_{n}$ and bipolar transistor current gains $\beta_{pnp}$ and $\beta_{npn}$) have been related to the structure geometrical features. Two-dimensional numerical simulations have also been extensively used in order to explain the most interesting features of the experimental data.

II. EXPERIMENTS

A. Structures

In order to analyze the influence of different layouts on CMOS latchup sensitivity, structures have been fabricated with the same process presenting the following main characteristics: starting bulk dopant concentration of $7 \times 10^{15}$ cm$^{-3}$ (p-type); n-well junction depth and peak surface concentration of 2.7 $\mu$m and $4 \times 10^{16}$ cm$^{-3}$, respectively; $n^+$ and $p^+$ junction depths of 0.2 and 0.4 $\mu$m, respectively; boron field implant in the substrate regions outside the active areas (with a surface concentration of $6 \times 10^{16}$ cm$^{-3}$).

Different sets of devices have been designed for each layout solution to be examined. Within each set, a critical length ($X$) is varied: in some cases this is the distance between the $n^+$ emitter and the well mask edge ($X_w$) determining the base width of the lateral bipolar transistor (BJT); in others, the separation between the $p^+$ emitter and the well mask edge ($X_p$) has been used as variable parameter. Furthermore, two complete sets of reference structures (without rings or buttied contacts) were fabricated to allow comparisons between different solutions. Altogether the following different layouts have been realized:

$L_1$ Reference solution, to study the vertical p-n-p characteristics.

$L_2$ Reference solution, to study the lateral n-p-n characteristics.

$L_3$ Featuring extra $p^+$ and $n^+$ diffusions with buttied contact in the well.


**Fig. 2.** Cross sections of the layout solutions considered in this work. All distances are in micrometers. Unless otherwise noted the p' and n' diffusions have $L=20 \mu m$ with a separation $D=10 \mu m$. The variable distances $X_e$ and $X_p$ and the distance ($Y$) between the emitters are also reported.

$L_4$ Featuring extra n' and p' diffusions with butted contact in the substrate.

$L_5$ Featuring extra diffusions with butted contacts both in the well and in the substrate.

$L_6$ Featuring an n' guard ring around the well.

$L_7$ Featuring a p' guard ring in the substrate surrounding the well.

Fig. 2 shows the device cross sections, while Table I gives a summary of the available structures. Unless otherwise stated, the length ($L$) and separation ($D$) of the p' and n' diffusions were 20 and 10 $\mu$m, respectively, while the device width (in the lateral direction) has been fixed at 200 $\mu$m.

**B. Experimental Procedure**

For the experimental part of this work, only static measurements have been performed. Thus, the triggering current ($I'$) [1] is defined as the dc current forced in the emitter of one of the two BJT's in order to initiate latchup, with the emitter of the other shorted to its base contact (substrate or well terminal). In this way $I'$ can be determined without ambiguity as the emitter current increases monotonically from the "off" to the "on" condition. Each test structure has been separately characterized with respect to current injection from both the p' and n' emitters. Since the current gains of the two bipolar transistors and the two base-emitter shunting resistances are quite different, naturally the results and the dependencies on the critical distances $X_e$ and $X_p$ obtained in the two cases are quite different.

The bipolar current gains ($\beta$) have been measured connecting the three transistor terminals only: the remaining emitter was left floating to avoid the undesired influence of latchup triggering as noticed in [5]. The shunting resistance has been determined with the same procedure indicated in [1].

Finally, measurements were also performed to characterize the structures in the holding condition, though this did not provide further information compared to the triggering experiments.

**III. Simulations**

Two-dimensional simulations, performed with the device analyzer PISCES-II [6], [7], have been extensively used to study potential, carrier concentrations, and current paths within the semiconductor. If simulations are to be used for accurate quantitative analysis, a global fitting procedure is needed to determine realistic parameter values (e.g., carrier lifetimes). In particular, since the current gains of the parasitic BJT's greatly affect latchup triggering characteristics, special care has been given to model the high injection regime. The considered models include Fermi–Dirac statistics, incomplete ionization (both affecting the injection efficiency of heavily doped emitters), and doping-dependent lifetimes. Furthermore, a bandgap-narrowing (BGN) model [8] different from that normally used as a default has been included in PISCES [9]. In our case, we have found that Slotboom's model for bandgap narrowing underestimates the emitter injection efficiency (regardless of the considered statistics) and leads to very low $\beta$ values. Consequently, such a model requires very long lifetimes in order to fit the experimental current gain in the low injection region. As a consequence, the enhanced minority-carrier charge in the base drives the transistor into the high injection regime at very low collector currents.
and $I'$ is largely overestimated. The Vol'tson model instead predicts a smaller BGN effect, leading to a higher $\beta_p$ fall-off knee current; thus, the experimental and simulated data can be matched using a minimum number of fitting parameters that all assume reasonable values. These values were obtained by fitting the $\beta$ versus $I_e$ curves for different $X_n$'s in different layouts. The resulting carrier lifetimes and the doping concentration in the expression of $[6]$ were: $\tau_{\text{ne}} = 1.8 \times 10^{-6}$ s, $\tau_{\text{pg}} = 1.0 \times 10^{-6}$ s, $N_{\text{eff}} = N_{\text{imp}} = 4 \times 10^{16}$ cm$^{-3}$.

Another crucial problem is due to the need to consider very large semiconductor areas in order to simulate real structures without distorting the current paths, thus heavily affecting the results. Furthermore, in the case of injection from the vertical p-n-p BJT's, the grid depth has been kept very large (70 $\mu$m) to make sure that the reflective boundary conditions imposed by the simulator do not affect the results. To check this point we assumed the criterion that the voltage drop along the bottom of the grid was never to exceed a few millivolts. The case of injection from the lateral n-p-n is less critical, and 40-$\mu$m-deep grids can be used. In any case, careful grid optimization was needed to handle large domains.

As an example, Fig. 3 shows the measured and simulated current gains of the vertical and lateral transistor versus the collector current in the case of the $L_3$ structure with $X_n = 4 \mu$m. Fig. 4, instead, shows the measured and simulated lateral transistor current gain of the $L_2$ and $L_3$ structures as a function of the distance $X_n$. As can be seen, good agreement between experiments and simulations has been reached over the whole $X_n$ and $I_e$ ranges, while differences are still observed at the low current regime of the transistors. This causes the simulated triggering currents to be different from measured ones, especially for those structures that have low $I'$ values (e.g., structure $L_1$ when triggered from the vertical p-n-p as shown in the next section). However, the above-mentioned discrepancy only slightly affects the other simulation results; in fact, most structures suffer latchup triggering at collector currents in the high injection region, where simulated and experimental results match together.

IV. RESULTS AND DISCUSSION: TRIGGERING CHARACTERISTICS

A. Reference Structures

We will discuss first the case of injection from the vertical p-n-p transistor. Fig. 5 presents the measured and simulated triggering currents for the $L_1$ structures. The emitter and collector currents at the triggering point ($I'_e$ and $I'_c$, respectively) show a weak dependence on the distance ($X_e$) between the p$^+$ emitter and the well mask edge, when $X_e > 2 \mu$m. This can be explained considering the p-n-p transistor as composed by a central vertical component, with constant base width (approximately 2.3 $\mu$m, coming from the difference between the well and the p$^+$ emitter junction depths), and by a lateral component whose base width is given by the sum of $X_n$ and the distance between the well mask edge and the effective junction (about 2.3 $\mu$m). For $X_e > 0$ the central transistor plays the dominant role, and $X_e$ does not affect the overall current gain. For $X_e = 0$ instead, the presence of the lateral component (with narrow base) increases the transistor $\beta$ and the triggering currents drop to a much lower value.

The low positive slope of the $I'_e$ curve has been observed also in the $L_2$ structures (when triggered from the same emitter), where the variable distance is that ($X_n$) between the n$^+$ emitter and the well mask edge.

Two-dimensional simulations of the substrate spreading resistance are sufficient to understand qualitatively this dependence (see Fig. 6). For increasing $X$, a fixed collector current $I$ spreads deeper in the substrate and it is collected more uniformly by the three vertical electrodes, thus decreasing the surface component of $I'_c$ that effectively triggers the lateral n-p-n BJT. Consequently, the collector current required to trigger the device increases with $X$.

As for the injection from the lateral n-p-n, no dependence of $I'$ on $X_n$ is found in the $L_1$ structures. This is reasonable since the characteristics of the lateral n-p-n are not affected by $X_n$, and the relevant current paths inside the well are mainly determined by the well depth, doping profile, and contact position.
This mode of triggering is instead, strongly affected by the distance \( X_n \), closely related to the n-p-n base width. In the experiments the \( L_2 \) structures at triggering show an approximately constant collector current (from 2.2 to 2.9 mA), while the emitter \( I' \) increases substantially from 2.9 to 6.0 mA due to the decrease in the lateral transistor current gain.

These results show that, at least for our bulk technology, \( X_n \) has little effect on the triggering process from the lateral n-p-n transistor (just as \( X_n \) when latchup is induced from the vertical p-n-p device). For this reason, in the remaining structures \( X_n \) will be kept fixed.

**B. Structures with Butted Contacts**

Butted contacts consist in the direct metal connection of contiguous p' and n' diffusions and are relevant for latchup since they lead to reduced base-emitter shunting resistance of the parasitic bipolar. In our test pattern the \( L_1, L_4 \), and \( L_5 \) structures (see Fig. 2) implement this type of solution at the source of the p- and/or n-channel MOSFET’s. These devices can operate in two different ways, depending on whether the large emitters (B) are connected or left floating. In the former case, the narrow emitters (A) butted to the well or substrate contact diffusion are always reverse biased (due to their low shunting resistance) and the layouts differ from the reference ones only for the swapping of the well and/or substrate terminals. In the other case, instead, the well (\( L_1 \) and \( L_4 \)) or substrate (\( L_4 \) and \( L_5 \)) contact diffusions act as real butted contacts. Let us consider first the case \( L_5 \), with the well contact butted to a narrow p' emitter (A) and a second 20-μm-wide p' emitter (B).

With this latter connected to the well contact, the structure differs from \( L_2 \) only for the swapping of the well and p' emitter contacts. This leads to a reduction of the well shunting resistance (\( R_w \)), thus enhancing the immunity to latchup induced by current injected through the n' emitter. In fact, a four-fold increase in \( I_{on} \) compared to \( L_2 \) is measured (see curves a and b in Fig. 7).

However, the most interesting and rather surprising feature of the data is the non-monotonic dependence of \( I_{on} \) on \( X_n \) indicating that, contrary to what is normally assumed, in this case wider structures can be more sensitive to latchup. This behavior results from two competing effects: 1) the effective \( R_w \) increases with \( X_n \) (that is a characteristic length of the substrate and not of the well) and 2) \( \beta_{n'p} \) lowers for increasing \( X_n \). In particular, the increase in \( R_w \) dominates for small \( X_n \) and determines the negative slope of \( I_{on} \), while at large \( X_n \) (hence \( I_{on} \)), the variation in \( \beta_{n'p} \) becomes the major effect.

This can be seen in Fig. 8 (a), (b), which shows the simulated current distributions for two \( L_3 \) structures with extreme \( X_n \) values (4 and 22 μm, respectively). The devices were driven with the same n' emitter current \( I_{on} \), close to the triggering point. Each line in the figures delimits a portion of the semiconductor containing 10 percent of the total current. The narrower structure (Fig. 8(a))
Fig. 8. Current flowlines for the I_n structures with (a) X_n = 4 μm and (b) X_n = 22 μm in the case of injection from the lateral n-p-n transistor. Each line represents 10 percent of the total current. The devices are driven with the same n' emitter current I_e close to the triggering point.

shows a much higher gain of the lateral n-p-n resulting in less current lines coming from the p' base contact and more from the n-well collector. However, most of the n-p-n collector current I_n crosses the substrate–well junction laterally and does not contribute to forward bias the p' emitter. On the other hand, the wider structure exhibits a lower β_npn but a larger portion of I_n crosses the well–substrate junction vertically, thus triggering the p-n-p transistor.

The result of these two competing effects is a slightly higher I'_{en} for the narrower structure (see Fig. 7).

The situation is shown in Fig. 9(a) where the n-p-n collector current (I_{cn}) is divided in two components, I_{cnl} and I_{cnr}, among which only the latter is responsible for latchup triggering. The simulated I_{cn} along the bottom edge of the well (ξ axis in Fig. 9(a)) is shown in Fig. 9(b): the two curves refer to extreme X_n values and to the same total current I_{cn}. As I_{cn} increases with X_n (while I_{cnl} decreases), for larger X_n, the critical forward bias of the emitter–base junction (V'_{ep}) is obtained for lower I_{cn}. As the triggering voltage V'_{ep} is almost constant, this effect can also be regarded as an increase of R_w with X_n.

Therefore, I'_{en} decreases with X_n as a consequence of increasing R_w, while I'_{en} first increases and then decreases as the reduction of β_npn is more important than the increase in shunting resistance.

The explanation given above can also be put in a mathematical form by means of a simple analytical model. In fact

\[
I'_{en} = \alpha_n \frac{I'_{en}}{\alpha_n} \frac{V'_{sp}}{R_w} \left[ \frac{1}{\beta_n} + \frac{1}{\beta_{n'p}} \right].
\]

(1)

Thus, assuming V'_{ep} to be constant and differentiating (1) with respect to X_n, we obtain

\[
\frac{dI'_{en}}{dX_n} = \frac{V'_{sp}}{R_w} \left[ -\frac{1}{\beta_{n'p}} + \frac{dR_w}{dX_n} \frac{1}{\beta_n} + \frac{1}{\beta_{n'p}} \left( -\frac{d\beta_n}{dX_n} \right) \right].
\]

(2)

For small values of X_n, β_{n'p} is large and R_w small; thus, the negative term in (2) dominates, while for larger X_n (smaller β_{n'p} and larger R_w), the positive term dominates.
The experimental data also show a local maximum of $I_{ce}'$ probably due to the sudden decrease of $d \beta_{pp} / dX_{n}$ just around $X_{n} = 10 \mu m$ (see curve a of Fig. 4): as a consequence the first term in (2) tends to dominate again, and $I_{ce}'$ decreases. In spite of its simplicity, the model of (1) with the measured values of $\beta_{pp}$ and $R_{w}$ for the $L_{3}$ case (Table II), reproduces the observed shape of the measured $I_{ce}'$ versus $X_{n}$ curve with good accuracy.

The corresponding simulations of the $L_{6}$ structures are also reported in Fig. 7: as can be seen, they reproduce the main features of the data for both $I_{ce}'$ and $I_{ce}''$ over a wide range of $X_{n}$, but fail to show the local peak of $I_{ce}'$. Qualitatively similar dependencies are obtained in experiments where the wide p⁺ emitter is left floating so that the well contact acts as a real butted contact, although the triggering currents increase significantly due to the reduced $R_{w}$, as shown in Fig. 7 (curves c and d).

As for the case of injection from the large p⁺ emitter, only a small improvement is observed due to the narrow p⁺ emitter acting as a pseudo-collector for the injected holes. $I_{ce}'$ increases with $X_{n}$ from 8.1 to 9.2 mA, compared to 6.6 and 8.1 mA for the $L_{2}$ reference structures.

Let us now consider devices with butted n⁺-p⁺ diffusions in the substrate (case $L_{4}$ in Fig. 2). When these structures are current driven from the p⁺ emitter with the wide n⁺ diffusion (B) either connected to the substrate contact or floating, the triggering current $I_{tp}$ ranges from 5.9 to 7.6 mA and from 9.5 to 13.0 mA, respectively. Only a small improvement in latchup resistance is observed as the p-n-p collector current spreads very deep in the substrate, thus making the resulting shunting resistance rather insensitive to the contact position at the surface.

On the contrary, this structure behaves much better if latchup is induced from the wide n⁺ emitter (B), due to the presence of the narrow n⁺ pseudo-collector in the substrate. In this case our $I_{ce}'$ is found to range from 7.1 to 14.2 mA.

Finally, n⁺-p⁺ butted diffusions were fabricated both in the well and in the substrate (case $L_{5}$), though these more complex structures do not exhibit any substantial improvement compared with the cases $L_{3}$ and $L_{4}$. If latchup is induced by current injection from the lateral n-p-n BJT, the $I_{ce}$ dependence on $X_{n}$ resembles that of the $L_{3}$ structures (Fig. 10) though the current values are much higher because of the reduction of the lateral transistor $\beta_{pp}$ caused by the n⁺ pseudo-collector.

As expected, $L_{5}$ and $L_{4}$ behave in the same way when triggered from the vertical p-n-p since neither $\beta_{pp}$ nor $R_{t}$ have substantially varied.

C. Structures with Guard Rings

Guard rings are circular p⁺ or n⁺ diffusions placed inside or outside the well [1]. The layouts $L_{6}$ and $L_{7}$ present the so called "majority-carrier guard rings" for electrons and holes, respectively, aimed at collecting the majority carriers injected across the well-substrate junction before they can forward bias the corresponding emitter. In the $L_{6}$ structures, the n⁺ guard ring is placed outside the well in order to collect electrons injected from the n⁺ emitter and entering the well, thus reducing the well shunting resistance.

Fig. 11 shows the experimental and simulated triggering currents $I_{ce}'$ and $I_{ce}''$ obtained in the case of injection from the lateral n-p-n transistor, for different values of $X_{n}$ and $W_{ge}$, the latter being the guard ring width. $I_{ce}'$ decreases with $X_{n}$ due to the same effect already described for the structures with butted contacts, $I_{ce}''$, instead, increases weakly with $X_{n}$ as a consequence of the combined effects of $X_{n}$ on $\beta_{pp}$ and $R_{w}$. Notice that at triggering the simulated $I_{ce}'$ is in excellent agreement with the experiments, while a considerable error (≈ 35 percent) is found in $I_{ce}''$. This discrepancy can be explained considering the difference between the simulated and measured $\beta$'s of the lateral n-p-n transistor reported in Fig. 3. In fact, because
of the high triggering currents found with the guard ring, the injecting transistor operates well into the high injection region, where $\beta$ is strongly dependent on the current level. Thus, small differences in the position of the knee in Fig. 3 (indicating the onset of the high injection regime) can lead to a strong reduction of the simulated $\beta$ and to overestimate the emitter triggering current.

However, the presence of the well guard ring does not improve the latchup resistance when the current is injected from the $p^+$ emitter: in our experiments, the emitter triggering current ranges from 7.4 to 8.6 mA for different values of $X_n$, which is about the same as with the reference structures.

The results for the case $L_7$, where a $p^+$ substrate guard ring surrounds the well, are given in Fig. 12 for the different values of $X_n$ and $W_{p^+}$, in the case of injection from the vertical p-n-p transistor. The ring collects the holes injected outside the well before they can bias the $n^+$ emitter junction, thus increasing the collector current required to trigger latchup. When the distance between the well and the ring increases, the substrate current flows more directly into the ring, and the portion of the collector current under the $n^+$ emitter decreases. Thus, $I_{tp}'$, and consequently $I_{tp}$, grow with $X_n$.

This effect can be clearly seen in Fig. 13(a), (b) showing the simulated current distributions for two different $L_7$ structures with $X_n = 4$ and 8 $\mu$m, respectively. As in the previous example ($L_5$), the two devices are current driven from the $p^+$ emitter and exhibit the same total current, while the narrower one is at the triggering point. In the wider structure more current lines (each delimiting 10 percent of the total current) flow directly into the ring so that more total current is required to trigger latchup.

Notice that the $p^+$ guard ring is the only scheme highly effective against triggering from the vertical p-n-p transistor. The improvement, however, is much less than that obtained with $n^+$ rings or butted well contacts in the case of injection from the lateral n-p-n because the p-n-p collector current spreads deeply in the substrate, thus making the value of the shunting resistance rather insensitive to layout solutions.

In the case of injection from the $n^+$ emitter, the $L_7$ structures do not show any improvement compared to the reference ones (for similar base widths).

**D. Summary of the Triggering Results**

To summarize the results of our triggering measurement, a comparison among the different layout solutions is presented in Fig. 14 for the case of injection from the lateral n-p-n. In order to evaluate the tradeoff between latchup hardness and area occupation, the emitter trigger-
The following conclusions can be drawn:

1) Strong latchup hardness is obtained only with the adoption of guard rings.

2) When the guard ring is present, latchup resistance is a strong function of its width and exhibits a much weaker dependence on the distance between the emitters.

3) In the structures with butted contacts the highest triggering currents are obtained with the shortest distance between emitter contacts.

Finally, because wide rings require large-area occupation, among our structures the best tradeoff is obtained for the \( L_6 \) structure with \( W_{gr} = 3.2 \mu m \) and \( X_n = 2 \mu m \).

V. RESULTS AND DISCUSSION: HOLDING CHARACTERISTICS

Fig. 15 summarizes the holding current measurements, here reported as a function of the distance \( Y \). The data for the structures \( L_3, L_4, L_5 \) have been obtained with the wide \( p^+ \) and \( n^+ \) emitters connected to the n-well and substrate terminals, respectively.

The results of these experiments are in substantial agreement with those presented in the triggering section. The structures with guard rings exhibit the highest latchup immunity; in particular, those with \( I_H > 100 \) mA can be considered practically latchup free because of the limitations in the power supplies used in real circuits. As in the triggering case, latchup hardness is a strong function of the ring width and of the distance \( Y \) between the two emitters.

In the structures with butted contacts the sustaining characteristics are qualitatively similar to the triggering ones: Fig. 15 shows that, in the \( L_3 \) structures, \( I_H \) monotonically decreases with \( X_n \) due to the increase in \( R_w \) (see the related discussion in Section IV). Finally the \( L_4 \) and \( L_5 \) devices exhibit holding characteristics similar to the case of \( L_3 \).

The holding voltage \( (V_H) \), instead, showed rather weak dependencies both on the distance \( X_n \) and on the layout solution as it ranges from 0.9 to 1.1 V in the reference
Fig. 15. Holding currents versus the distance $Y$ between the emitters for the structures $L_2$, $L_1$, $L_0$, with $W_{em} = 3.2$ (△), 6.4 (○), and 12.8 μm (*), and $L_0$ with $W_{em} = 3.2$ (■), 6.4 (▲), and 12.8 μm (●).

layouts ($L_1$ and $L_2$), from 1.2 to 1.4 V in the case of butted contacts ($L_3$, $L_4$, and $L_5$), from 1.6 to 2.5 V and from 1.3 to 2.0 V in the $L_6$ and $L_7$ structures, respectively.

VI. CONCLUSIONS

A detailed analysis of the layout dependencies of n-well CMOS latchup characteristics has been presented. Different layout solutions have been experimentally investigated both in the triggering and sustaining mode of operation. For each layout the dependence of latchup resistance on critical distances has been characterized.

The layout effectiveness in preventing latchup greatly depends on the triggering mode, namely on whether the vertical p-n-p or the lateral n-p-n is used as current injector. In the latter case, most of the parasitic current flows close to the surface, thus enhancing the role of the detailed surface configuration, while in the former the deep spreading of the current in the substrate makes latchup much less dependent on layout scheme.

Latchup triggering is rather insensitive to the distance $X_w$ while the dependence on $X_e$ is of some interest. In fact, two competing effects on $B_{on}$ and $R_n$ lead to a weak increase or non-monotonic dependence of $I_{on}$ on $X_e$ for structures with guard rings or butted contacts, respectively.

The best results in latchup hardness are obtained with the use of guard rings, especially if their width is sufficient. However, both n⁺ and p⁺ guard rings should be included to completely prevent latchup triggering from both bipolar transistors.

Finally, some conclusions can be drawn about the use of two-dimensional simulations. Careful modeling of the bipolar transistors and the use of very large grids allowed simulation of the realistic structures used in the experiments. The simulations confirmed the dependencies found experimentally, and quantitatively acceptable results were obtained with the same model parameters extracted from, and used for, a wide range of different structures and currents ranging over two orders of magnitude. Furthermore, the simulations allowed a detailed study of the current distribution in the substrate, in order to understand some un-

expected dependencies of the triggering currents on the device geometries.

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Roberto Menozzi was born in Genova, Italy, in 1963. He received the Laurea degree in electrical engineering from the University of Bologna in 1987. Since then, he has joined a research group at the University of Bologna, working in the field of electronic devices. In particular, he has worked on the characterization and study of latchup in advanced C-MOS technologies.

Luca Selmi was born in Rome, Italy, in 1961. He graduated in electrical engineering from the University of Bologna in 1986. Since then, he joined the Department of Electronics and Computer Science of the University of Bologna as a Research Assistant, working in the field of electronic devices. In particular, he has worked on the characterization and study of latchup in advanced C-MOS technologies.

Ermes Sangiorgi (S’85–M’85) was born in Faenza, Italy, in 1954. He received the Laurea degree in electrical engineering from the University of Bologna in 1979. In 1982, he was appointed as a Research Associate at the University of Bologna. In 1983 and 1984, he was a Visiting Scientist at Stanford University, CA, working on contact modeling and latchup-resistant CMOS technologies. Since 1985, he has been a consultant at AT&T Bell Laboratories, Murray Hill, NJ. In 1986, he was appointed Associate Professor in Applied Electronics at the University of Udine, Italy. His interests concern solid-state devices and integrated circuits. In particular, he has been working on silicon dioxide physics, hot-electron effects in MOSFETs, contact modeling, latchup in CMOS structures, and Monte Carlo device simulations.
Giuseppe Crisenza was born in Italy in 1950. He received the Doctor degree in physics from the University of Milan, Milan, Italy, in 1977. His doctoral work was a study of the optical and electronic properties of avalanche photodiodes.

In 1978, he joined the central R&D Department of ST Microelectronics (formerly SGS Microelettronica), Agrate, Italy. Since then, he has been working in the VLSI Process Development Group. Until 1978, he was engaged in NMOS nonvolatile memory process development, working on process architecture, high-voltage devices, memory-cell characterization, and new cell concepts. From 1985 to 1987, he led the CMOS EPROM process development for 1-Mbit generation. He is currently responsible for the development of CMOS processes for 1- and 4-Mbit EPROM's. He has filed two patents on EPROM processes.

Tiziana Cavioni was born in Verbania, Italy, on February 3, 1955. She received the degree in physics from the University of Pavia, Pavia, Italy, in 1979.

She obtained a one-year research (1978–1979) grant from C.C.R. Euratom-Ispra, Italy, to study radiation damage induced in a-SiO2 by light (α and β particles) and heavy (Ni5+) ion bombardment. Since graduating, she has been with the ST (SGS-Thomson Microelectronics) R&D Department, Agrate Brianza, Italy, where she worked on EEPROM projects, especially on thin oxide problems. She developed the isolation and well processes for 1-Mbit EPROM’s. She is currently working on an advanced CMOS process for 4-Mbit EPROM memory and is interesting in the latchup problems connected with CMOS high-voltage processes.

Bruno Ricció (M’85) was born in Parma, Italy, in 1947. He graduated in electrical engineering from the University of Bologna, Italy, in 1971 and received the Ph.D. degree from the University of Cambridge, United Kingdom, in 1975.

While at Cambridge, he worked at the Cavendish Laboratory. In 1980, he became a Full Professor of Applied Electronics at the University of Padova, Italy. In 1983, he joined the Department of Electronics of the University of Bologna, Italy. In 1981, he was a Visiting Scholar at the University of Stanford and, later, at the IBM Thomas J. Watson Research Center, Yorktown Heights, NY. His scientific interests concern solid-state devices and integrated circuits. In particular, he has worked on electron transport in polycrystalline silicon, tunneling in heterostructures, silicon dioxide physics, hot-electron effects in MOSFET’s, latchup in C-MOS structures, and Monte Carlo device simulation. He is also interested in circuit design and testing.

Dr. Ricció serves as the Associate Editor for Europe for the IEEE Transactions on Electron Devices.